EC2x&EG2x-G Series

PCB Design Guideline

LTE Standard Module Series

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About the Document

Revision History

Version	Date	Author	Description
1.0	2020-07-23	Lim PENG	Initial
1.1	2020-07-24	Lim PENG	Revised few typos.

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1 Introduction

This document mainly introduces the PCB reference design for Quectel LTE Standard EC2x&EG2x-G series modules, and it takes EC25-TE-A, FC20-TE-A and UMTS&LTE EVB as examples.

1.1. Applicable Modules

Table 1: Applicable Modules

Module Series	Module
EC2x series	EC21 series
	EC25 series
	EC20 R2.1
EG2x-G	EG21-G
	EG25-G

1.2. Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating EC2x&EG2x-G series modules. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, use emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength.
	The cellular terminal or mobile contains a transmitter and receiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs to turn off wireless devices such as mobile phone or other cellular terminals. Areas with potentially explosive atmospheres include fuelling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders.

2 PCB Design Overview

2.1. Footprint and Keepout Area

- A 4-layer PCB is strongly recommended.
- First, check whether the module's footprint is of the latest version provided by Quectel. For specific footprint of each module, please refer to ***document [1]***, ***[2]***, ***[3]*** or ***[4]***.
- Do not design pads 73–84 and do not route the keepout area with any traces or copper.

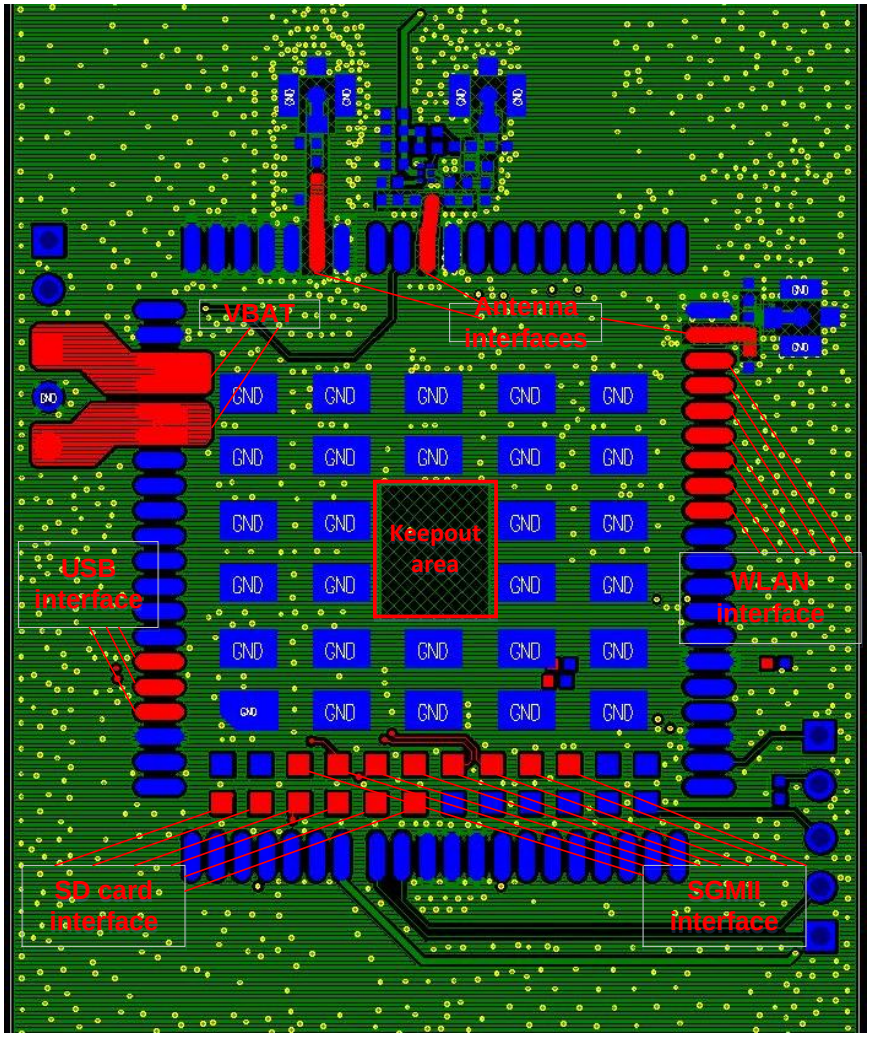

Figure 1: Overview of TE-A 1st Layer

2.2. Design Priorities and Considerations for PCB Traces

2.2.1. Design Priorities

Design priorities of PCB traces in order:

- Antenna traces.
- High-speed signal (SGMII, SDIO and USB) traces.
- Power supply (VBAT_BB, VBAT_RF, USIM_VDD, SDIO_VDD, VDD_EXT) traces.
- Other traces

2.2.2. Design Considerations

- The radiation of PCM interface and power supply could affect RF performance, so keep them away from RF signal traces and components.
- Drill as fewer vias as possible for high-speed signal traces (SGMII, SDIO and USB interfaces) since vias will affect the continuity of the impedance. Route the differential pair traces on the same layer.
- To minimize the signal return path, the GND vias for signals such as USB, SDIO, SGMII, PWRKEY and RESET_N should be close to the vias when the traces change layers.

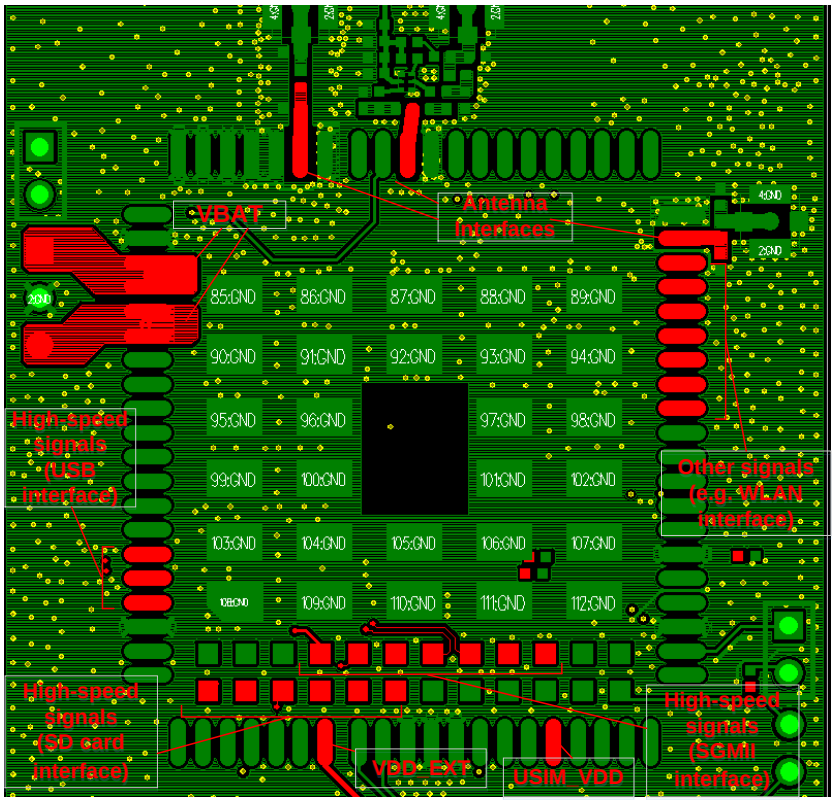

Figure 2: High-priority Signals to Be Designed (TE-A 1st Layer)

3 Interface Design

3.1. Power Supply

3.1.1. DC-DC Converter

- DC-DC converter should be away from the sensitive signal traces such as SDIO, USB, SGMII, audio and RF. If possible, shield DC-DC converter with shielding cover and reserve spacing for shielding frame.
- Place the capacitor and inductor for the DC-DC converter as close as possible to the corresponding pins of the DC-DC converter to minimize the loop area.
- Place output capacitors near input capacitors to share common ground area on outer layers.
- Provide adequate thermal relief area at the gound area on outer layers along with any additional inner ground planes.

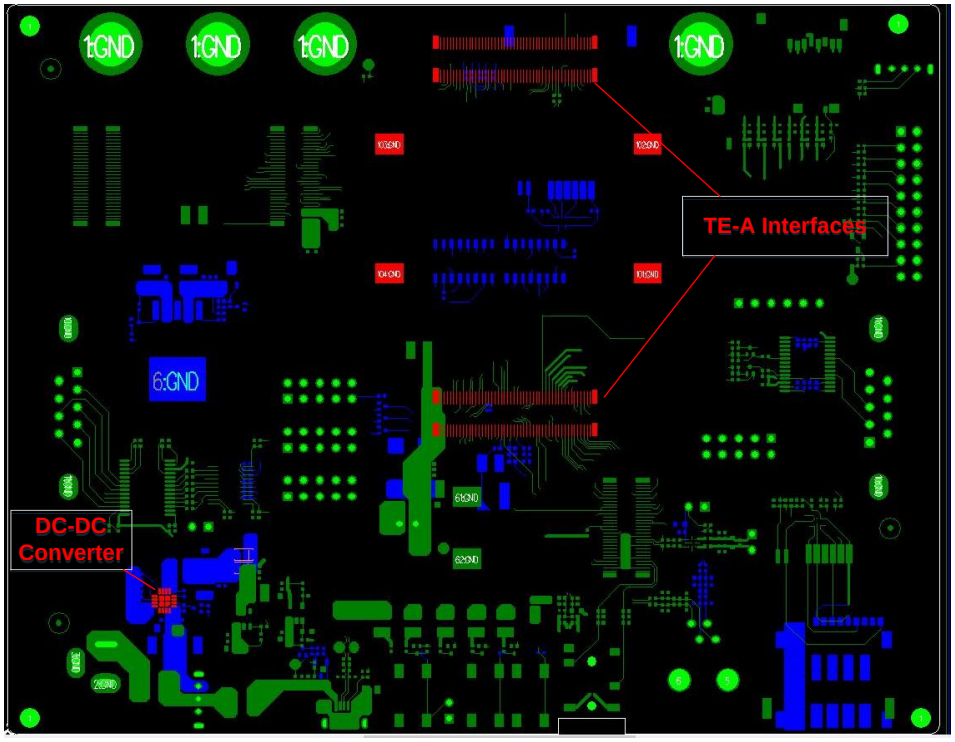

Figure 3: DC-DC Converter (EVB 4th Layer) and Module Interfaces On TE-A (EVB 1st Layer)

3.1.2. VBAT

- Place 100 μF, 100 nF, 33 pF and 10 pF capacitors for both VBAT_BB and VBAT_RF respectively. The smaller the capacitance is, the closer the compositors are to the two VBAT pins.
- The maximum current consumption of VBAT_RF is 1.8 A and its trace width is recommended to be no less than 2 mm. The maximum current consumption of VBAT_BB is 0.8 A and its trace width is recommended to be no less than 1 mm. Moreover, please pay attention to the capability and quantity of vias in the traces. The GND vias of the filter capacitors for VBAT should be drilled down to the nearest main ground.

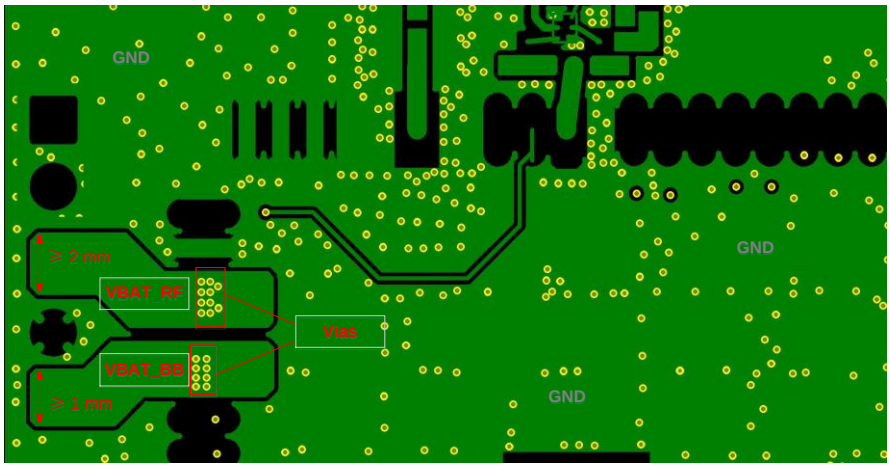

Figure 4: VBAT Traces (TE-A 1st Layer)

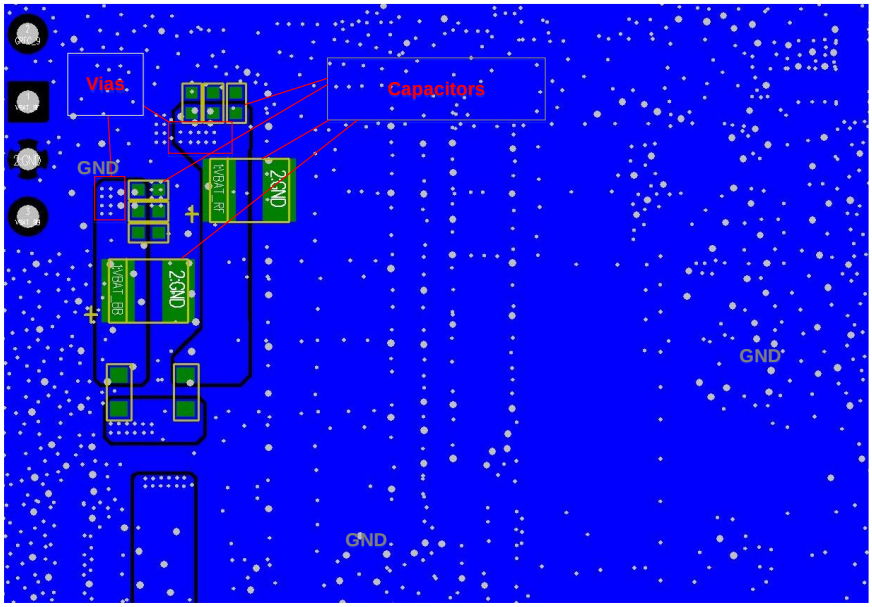

Figure 5: Traces of VBAT with Capacitors (TE-A 4th Layer)

- TVS for VBAT should be placed close to module's pin VBAT_BB and VBAT_RF.
- VBAT traces should be away from sensitive signal traces such as SDIO, USB, SGMII, USB audio and RF to reduce the risk of cross-talk.
- A layer with VBAT traces and reference ground plane is recommended. When a power plane is used, a complete ground plane should be added in adjacent layer as the reference plane.

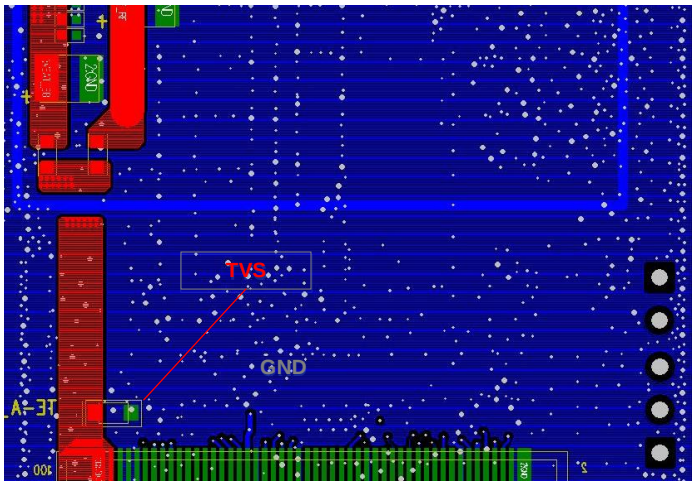

Figure 6: Traces of VBAT with a TVS (TE-A 4th Layer)

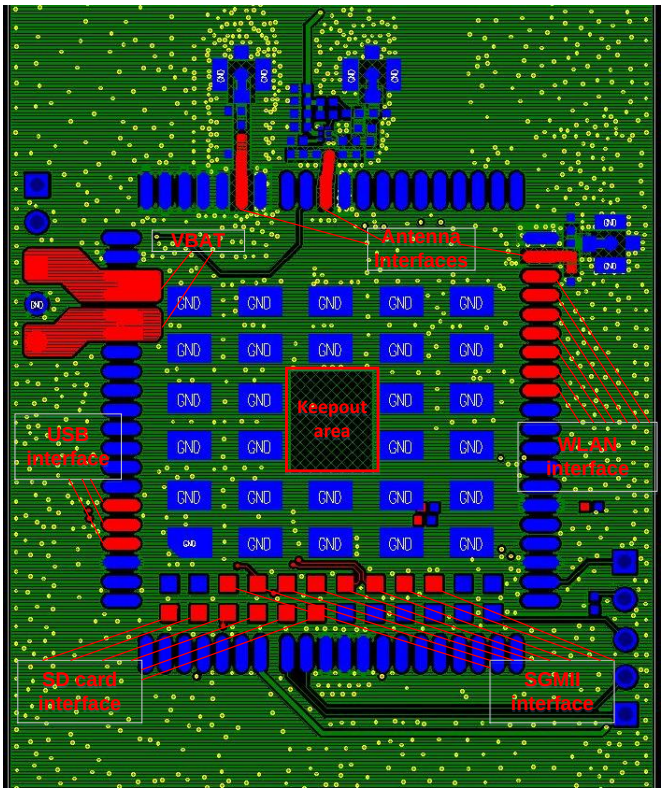

Figure 7: VBAT & Sensitive Signal Traces (TE-A 1st Layer)

3.2. PWRKEY & RESET_N

- PWRKEY and RESET_N signal traces are recommended to be surrounded with ground.
- If filter capacitors for PWRKEY and RESET_N are required, put them near the two pins.

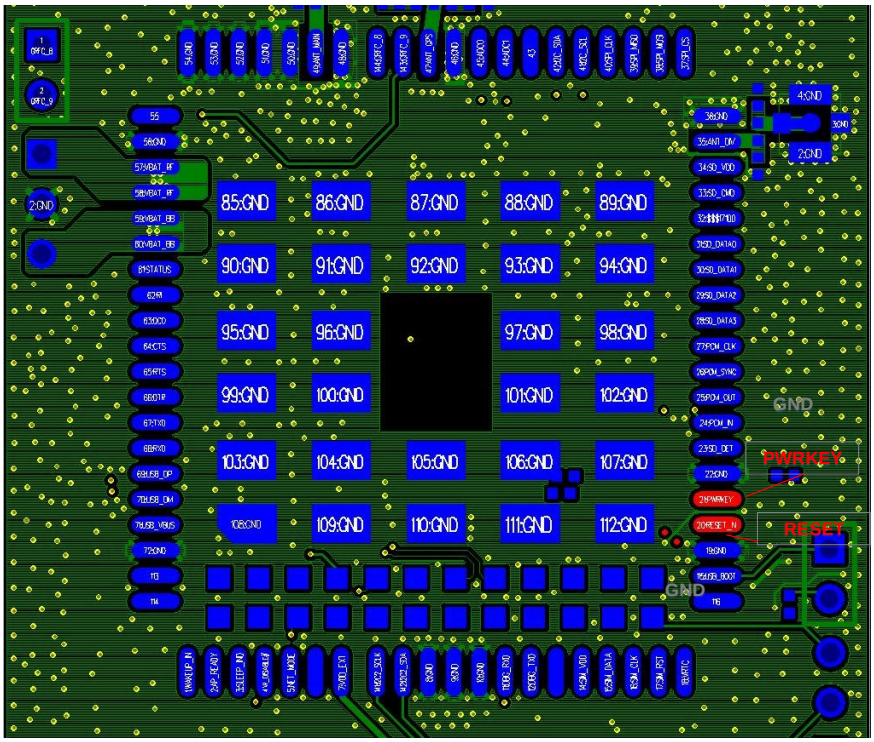

Figure 8: PWRKEY and RESET_N Traces (TE-A 1st Layer)

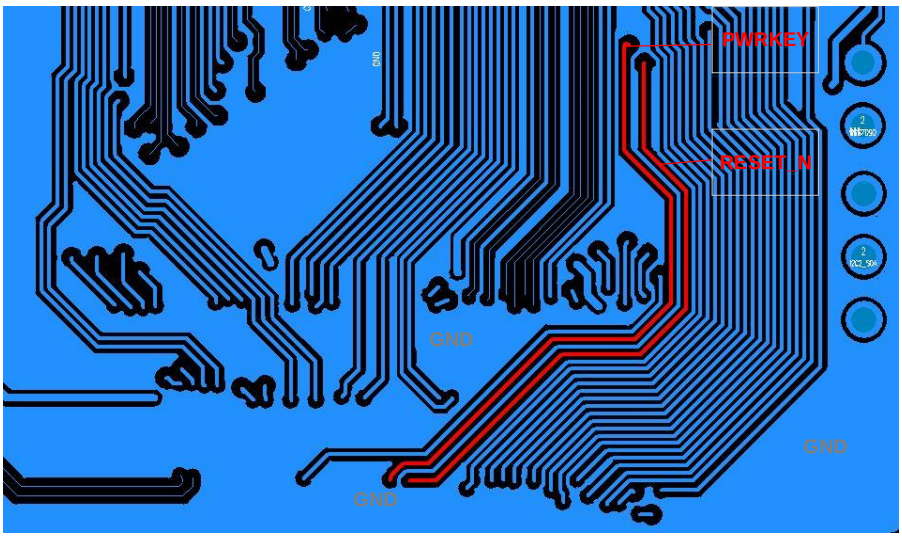

Figure 9: PWRKEY and RESET_N Traces (TE-A 3rd Layer)

3.3. USB Interface

3.3.1. USB_DM & USB_DP Signals

- The spacing between USB_DP/USB_DM and other signal traces should be greater than 0.5 mm, maintaining the integrity of the reference plane and avoiding crossing with signal lines on adjacent layers.
- USB_DP and USB_DM are recommended to be routed on the inner layer, with the differential impedance controlled to 90 Ω. Keep the spacing and length between traces comparatively equal, with the length tolerance less than 2 mm and the total length less than 120 mm.
- When a TVS needs to be added for USB_DP and USB_DM signal traces, it should be close to USB connector and the junction capacitance of the TVS should be less than 2 pF.

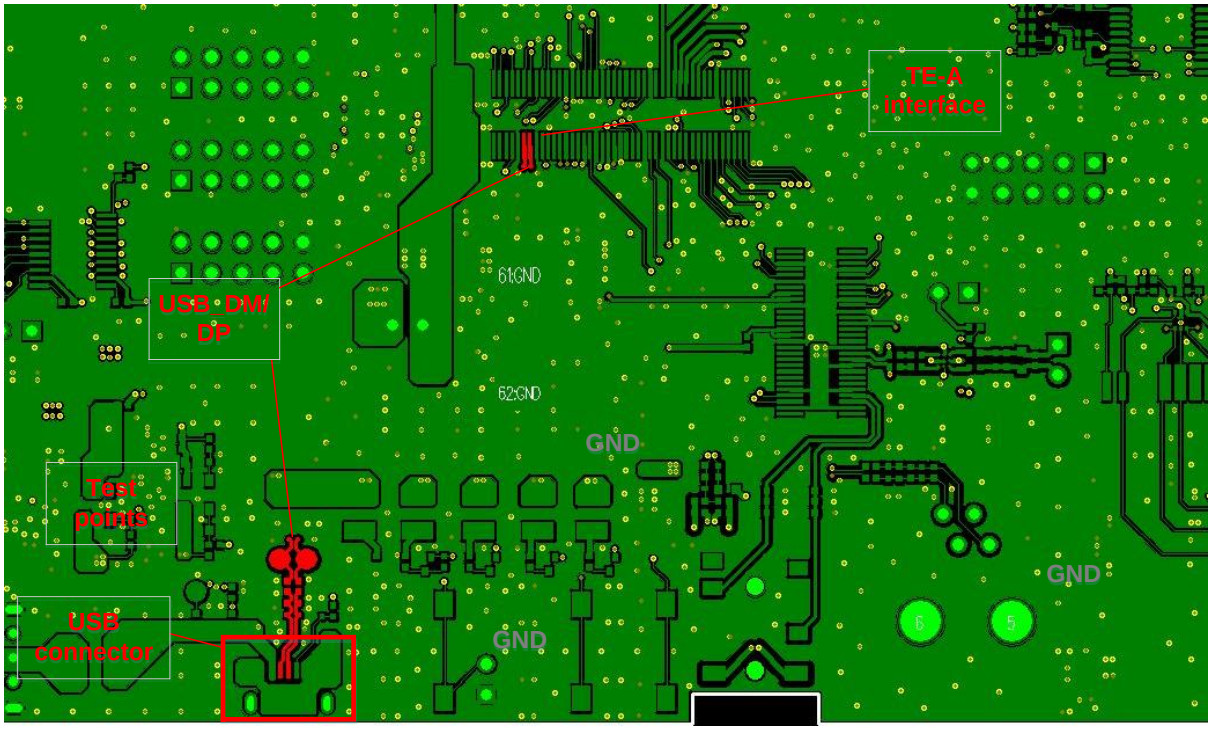

Figure 10: Overview of USB_DM/DP Signal Traces (EVB 1st Layer)

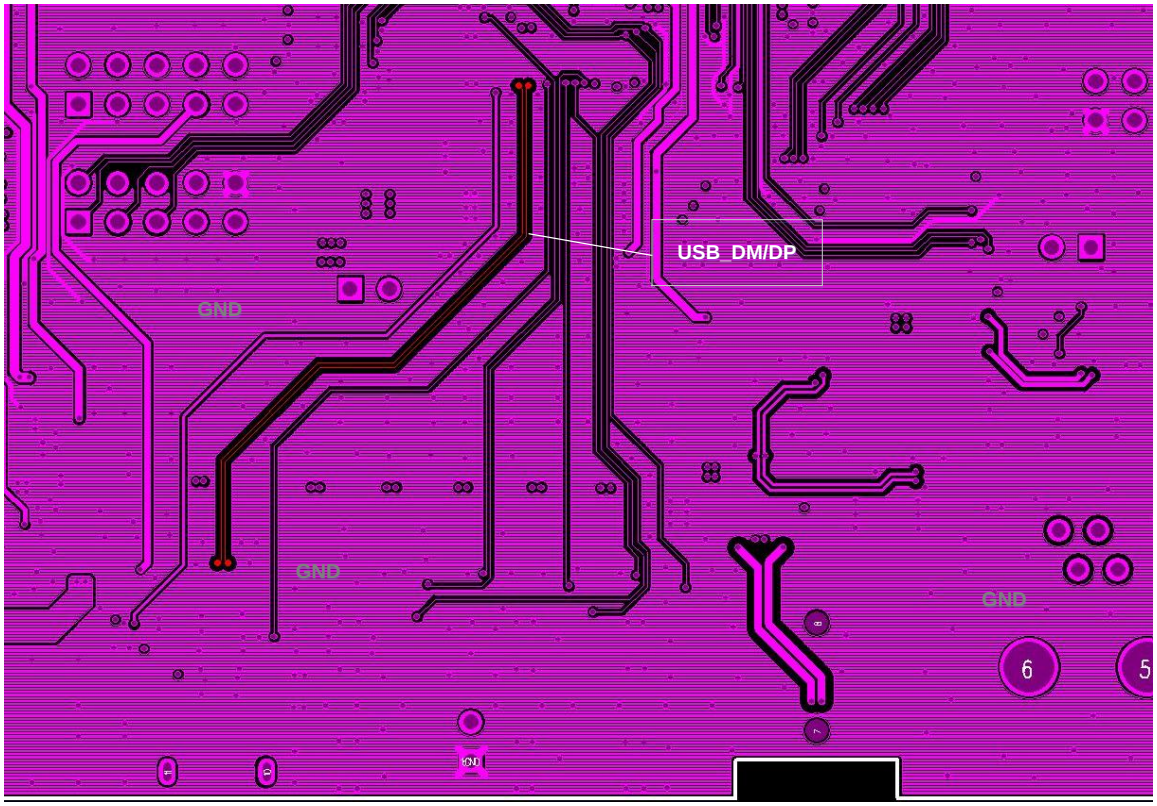

Figure 11: Overview of USB_DM/DP Signal Traces (EVB 3rd Layer)

3.3.2. USB_VBUS Signal

USB_VBUS is a USB detection signal, with maximum current of 1 mA. In general, a trace width of 0.1 mm is sufficient.

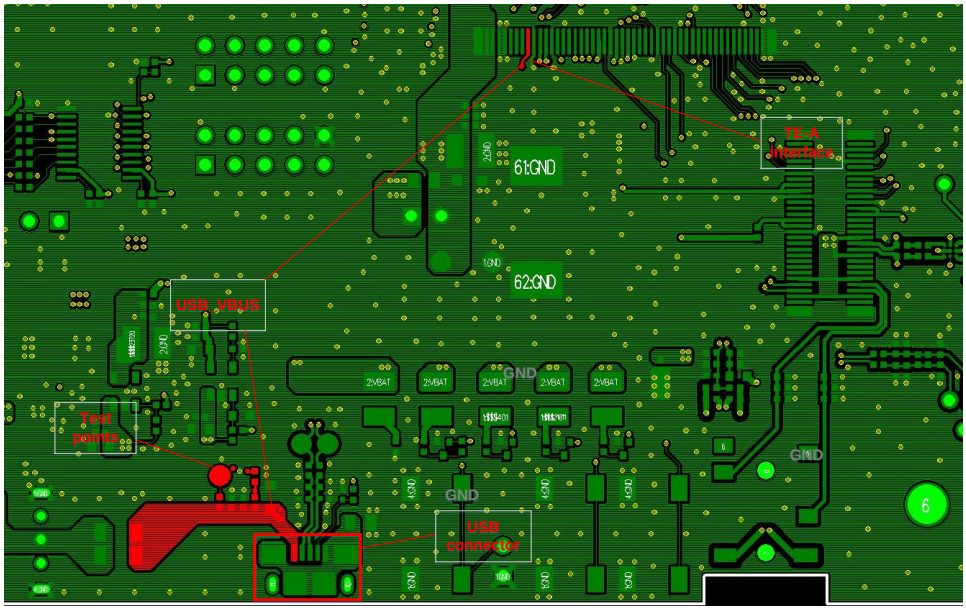

Figure 12: Overview of USB_VBUS Signal Trace (EVB 1st Layer)

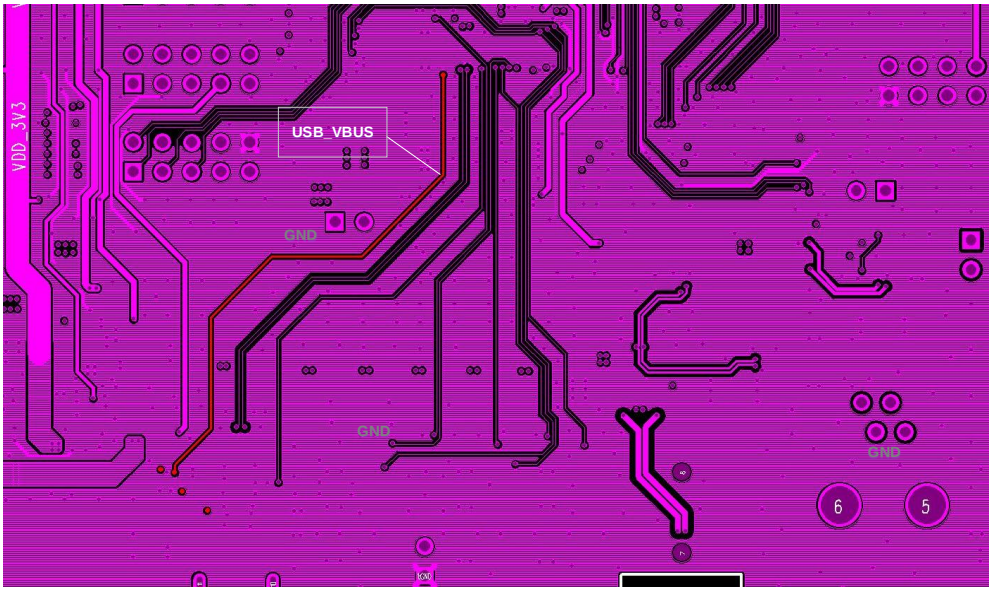

Figure 13: Overview of USB_VBUS Signal Trace (EVB 3rd Layer)

3.4. Ethernet PHY

3.4.1. SGMII Interface

- Signal traces of SGMII_MCLK, SGMII_MDATA, EPHY_RST_N and EPHY_INT_N should be surrounded with ground.
- The spacing between SGMII_TX_M/SGMII_TX_P/SGMII_RX_M/SGMII_RX_P lines should be at least 3 times wider than the traces, and that between the SGMII signal trace and other signal traces should also be at least 3 times wider than SGMII traces.
- Keep the maximum length of the SGMII signal traces less than 10 inches and the difference between signals of the differential pairs (SGMII_TX_P and SGMII_TX_M, SGMII_RX_P and SGMII_RX_M) less than 20 mil.
- The differential impedance of SGMII signal traces is 100 Ω ±10 %, and the reference ground of the area should be complete.
- The series capacitors for SGMII_TX_M/SGMII_TX_P should be close to PHY component, while the series capacitors for SGMII_RX_M/SGMII_RX_P should be close to the two pins.

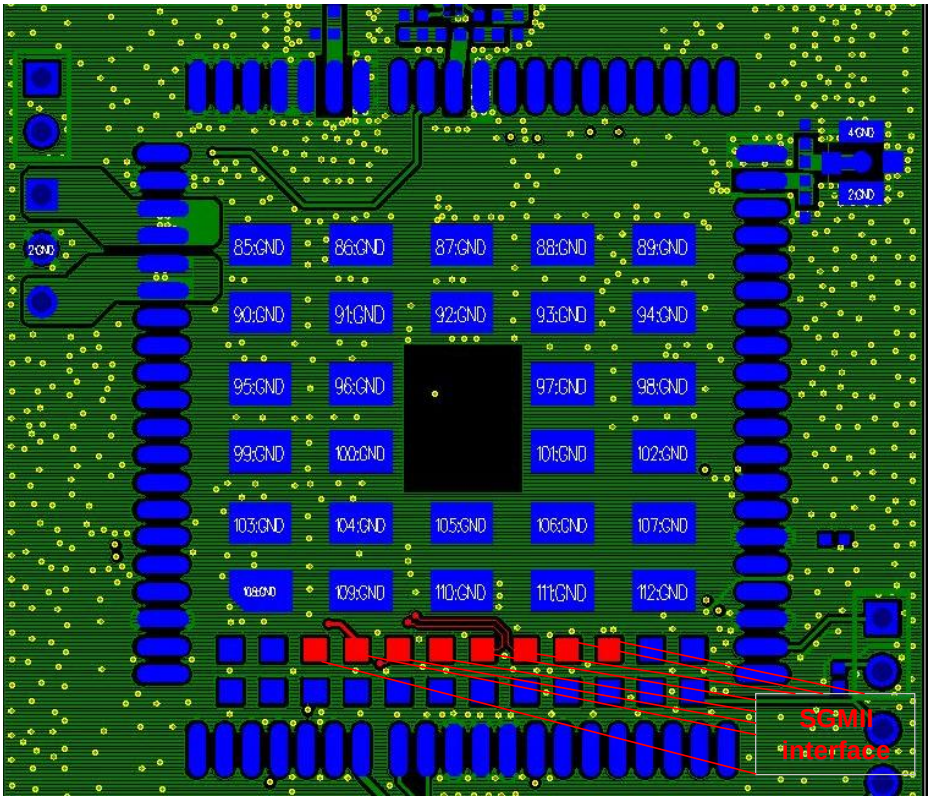

Figure 14: Overview of SGMII Signal Traces (TE-A 1st Layer)

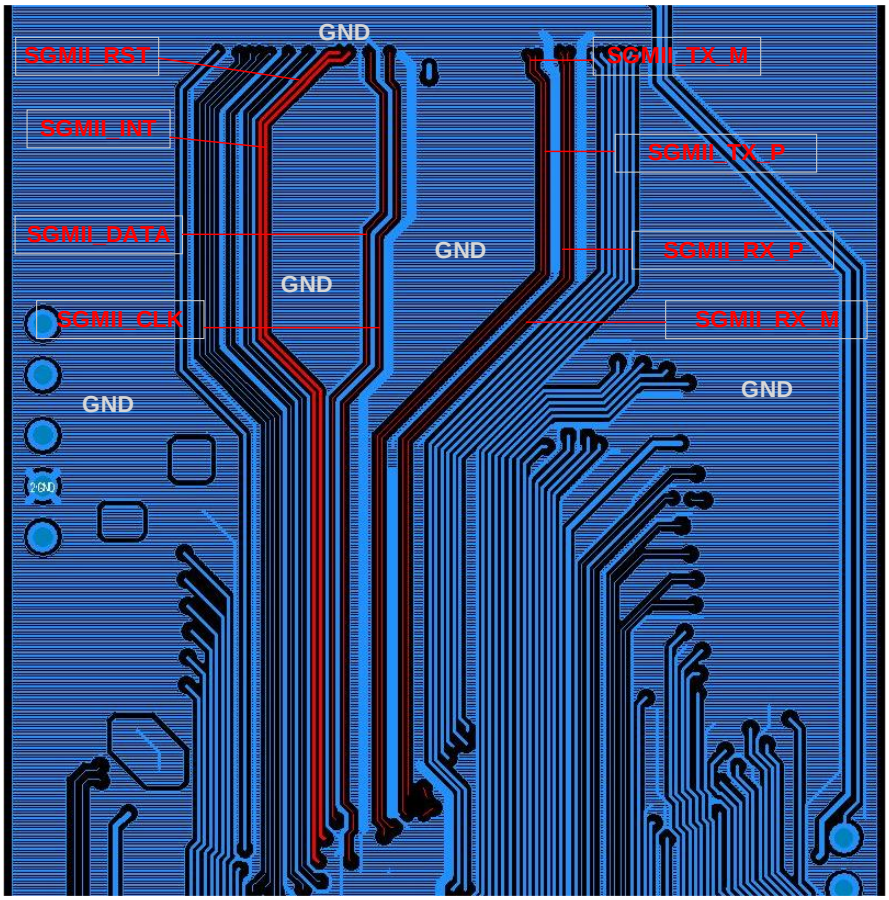

Figure 15: Overview of SGMII Signal Traces (TE-A 3rd Layer)

3.4.2. Ethernet Components

A four-layer PCB should be used when using the SGMII interface to implement the Ethernet function in the application.

- The first layer is for non-sensitive traces and 1.1 V power supply traces.
- The second layer is strongly recommended for 3.3 V and 2.5 V power supply traces and ground plane.
- The third layer should be a reference ground.
- The fourth layer is used for main signal traces.

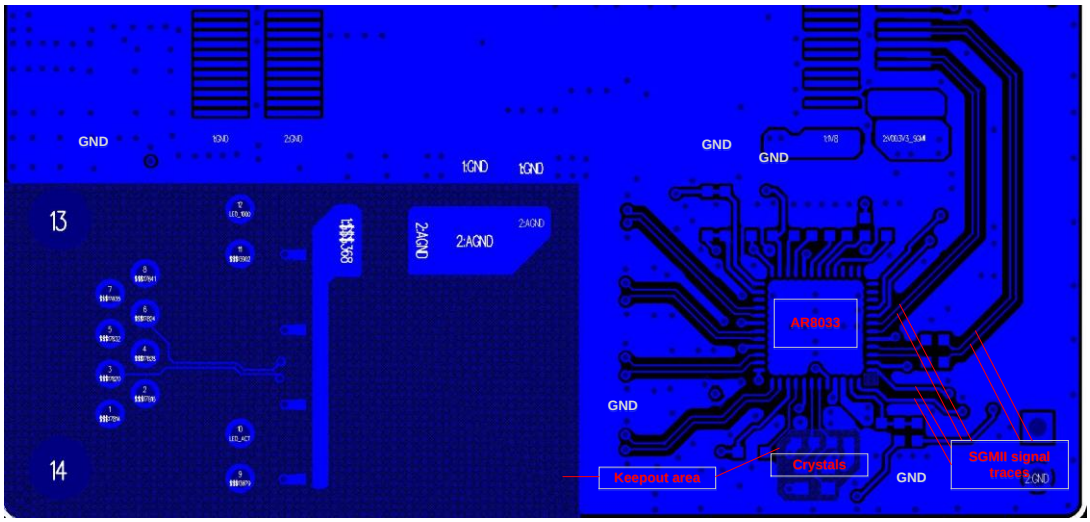

Figure 16: Recommended PCB Layout of SGMII Interface (TE-A 4th Layer)

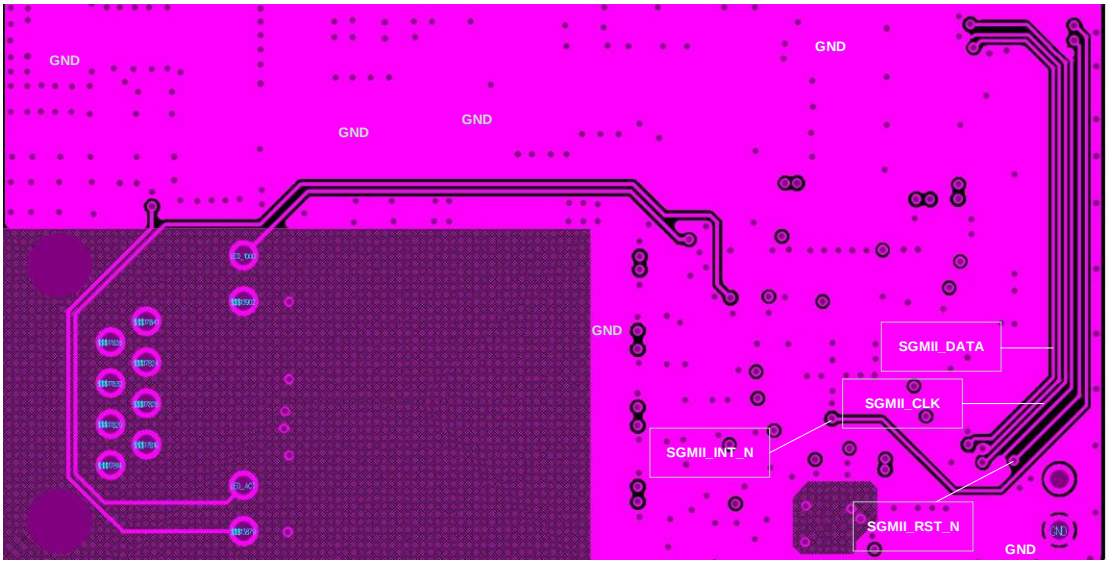

Figure 17: Recommended Reference PCB Layout of SGMII Interface (EVB 3rd Layer)

DVDD_1V1 is output by AR8033's LX pin through an LC circuit. The 4.7 μH inductor in the LC circuit should be able to provide 1 A current with low direct current resistance. The trace width for the inductor is recommended to be at least 1 mm. Besides, there is a reference ground plane needed for inductance isolation near the 4.7 μH inductor The following figure shows the recommended inductor placement as well as trace routing and trace width for AR8033 pins.

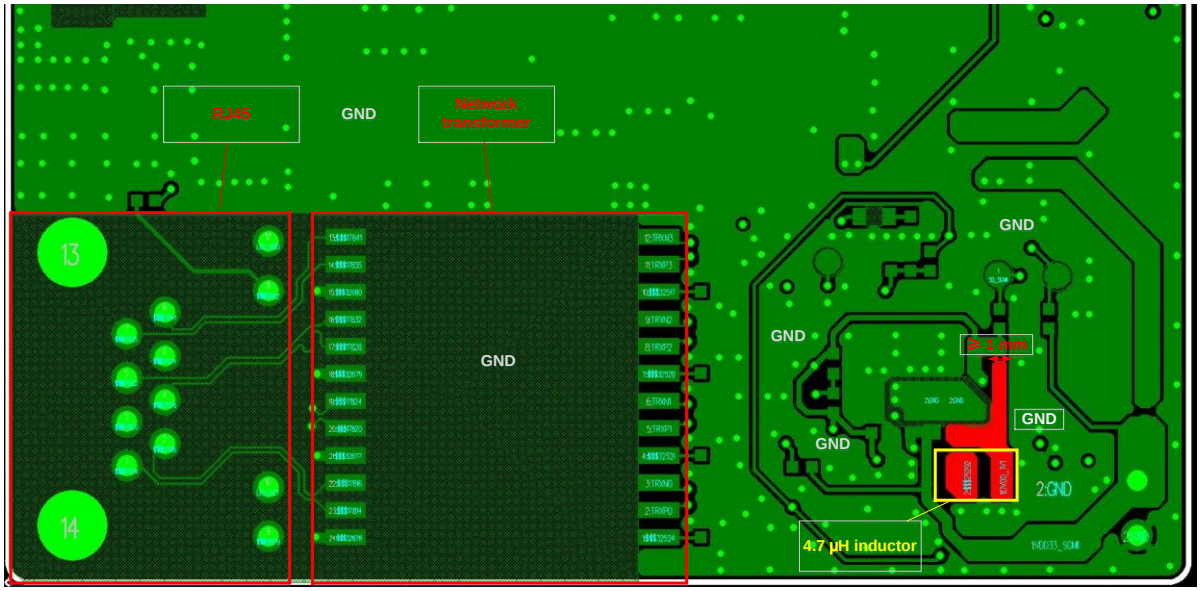

Figure 18: Layout of Recommended 4.7 μH Inductor, GND and Traces of AR8033 (EVB 1st Layer)

3.5. Audio Interfaces

3.5.1. PCM Interface

- The filter capacitors for PCM_CLK/PCM_SYNC should be placed close to the two pins.
- The PCM bus is recommended to be routed on inner layers, and it is recommended that each trace be surrounded by ground traces separately. If there are limits of space, at least ensure PCM_CLK is surrounded by ground traces, and other three signal traces can be surrounded together by ground traces.
- PCM traces should be kept away from interference sources such as clock, RF, crystals, power supplies, etc.

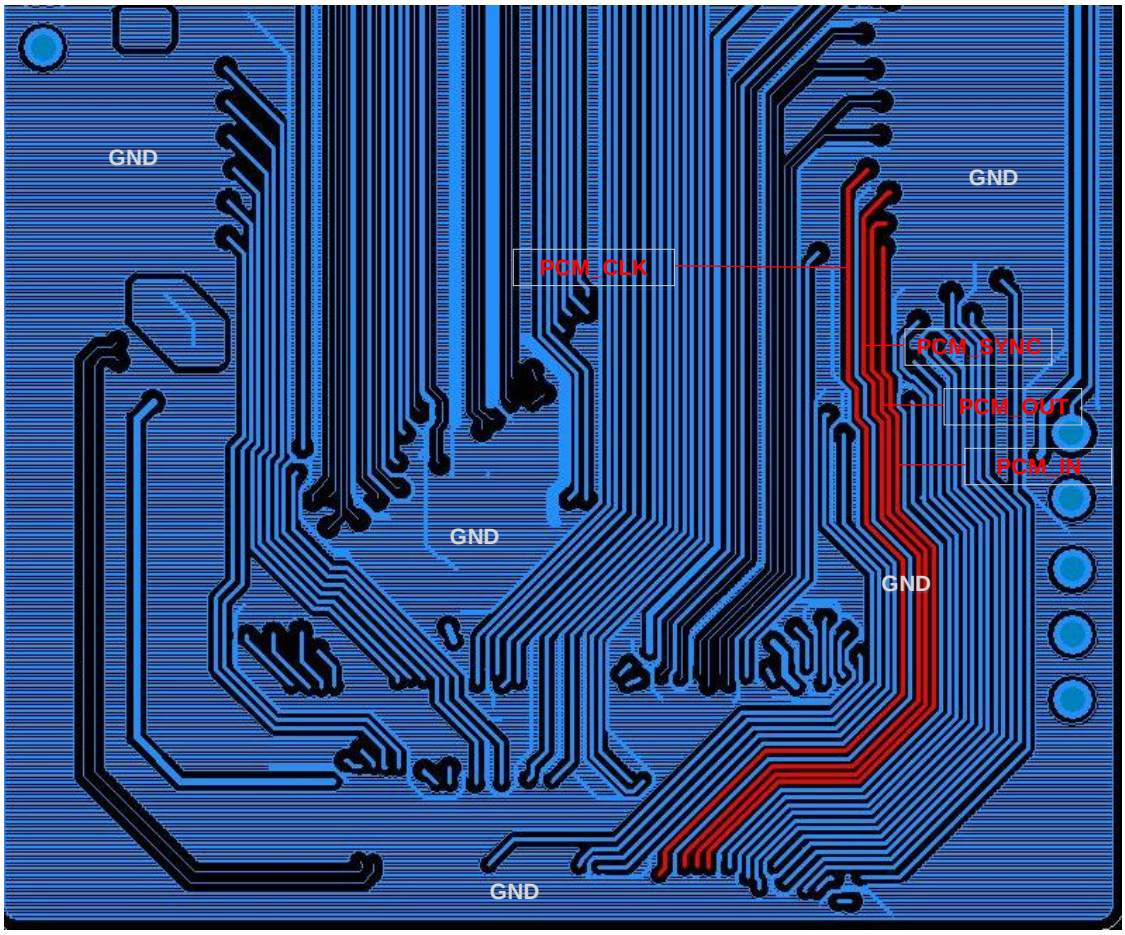

Figure 19: Overview of PCM Signal Traces (TE-A 3rd Layer)

3.5.2. Codec & Microphone & Speaker

The codec should be kept away from interference sources such as high-power components, power sources, CPU, DRAM, Flash, PMU, LCD, RF antennas and other high-frequency components, isolated, and close to one of the edges or corners of the board, and could be shielded if there is sufficient space.

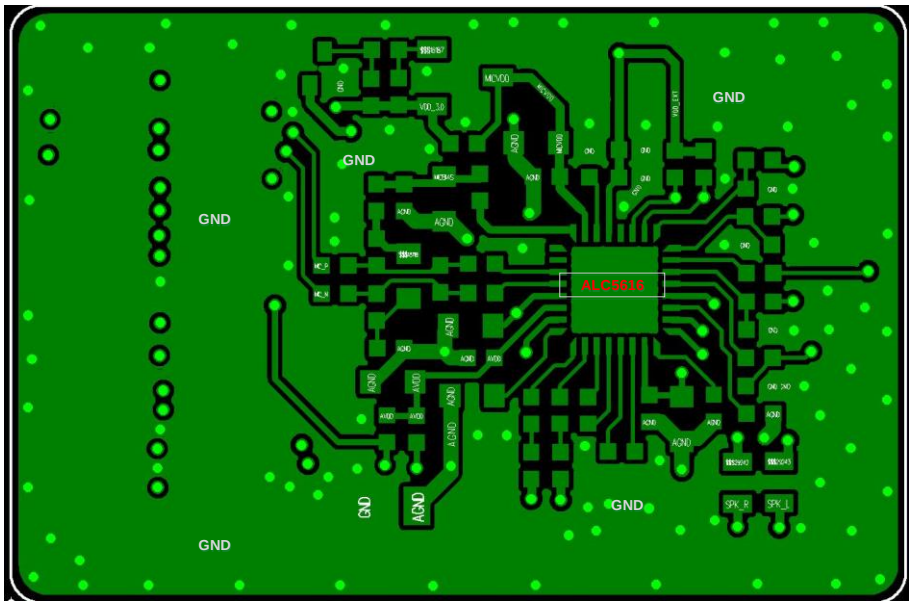

Figure 20: Overview of Codec ALC5616 (EVB 1st Layer)

- Keep the traces for microphone and speaker as short as possible. For MIC signals, it is recommended to design differential pairs.
- The analog output could only be capable of driving earphone and headset. For larger power loads such as loudspeakers, an audio power amplifier should be added in the design.
- All MIC and SPK signal traces should be routed with total grounding and far away from interference sources.
- The spacing between MIC_P and MIC_N should be more than 0.25 mm. To avoid cross-talk, the spacing between the differential pair traces should exceed 1.5 mm. To avoid interference between different MIC traces, MIC1 and MIC2 traces should be routed on different layers as much as possible.
- For signal traces of speaker, the length should be more than 0.5 mm and requires low impedance.
- The reference ground for microphone, speaker and MICBIAS should be analog ground while for PCM interface should be digital ground. Besides, pay attention to the integrity of the analog signal reference plane.

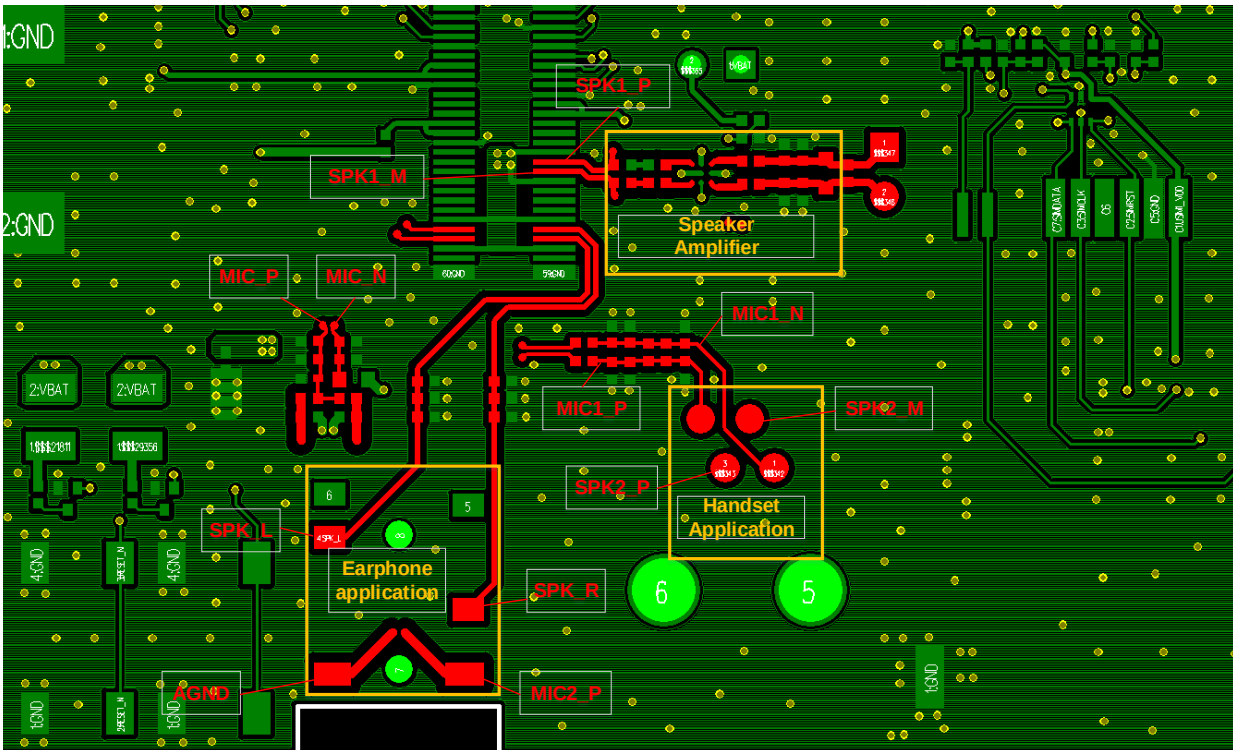

Figure 21: Overview of Analog Audio Signal Traces (EVB 1st Layer)

3.6. SD Card Interface

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
- Keep the impedance of SDIO signal traces at 50 Ω ±10 %, maintaining the integrity of the reference plane. SD_CLK and SD_CMD should be surrounded with ground on the layer and ground planes above and below. If limited by space, the SD_DATA0 to SD_DATA3 could be surrounded with ground together.
- The total length of each SDIO signal trace should be less than 50 mm, and the difference between them should be less than 1 mm.
- The load capacitance for SD card signals should be less than 15 pF.
- If a SD card is applied, a TVS should be placed close to the SD card connector.

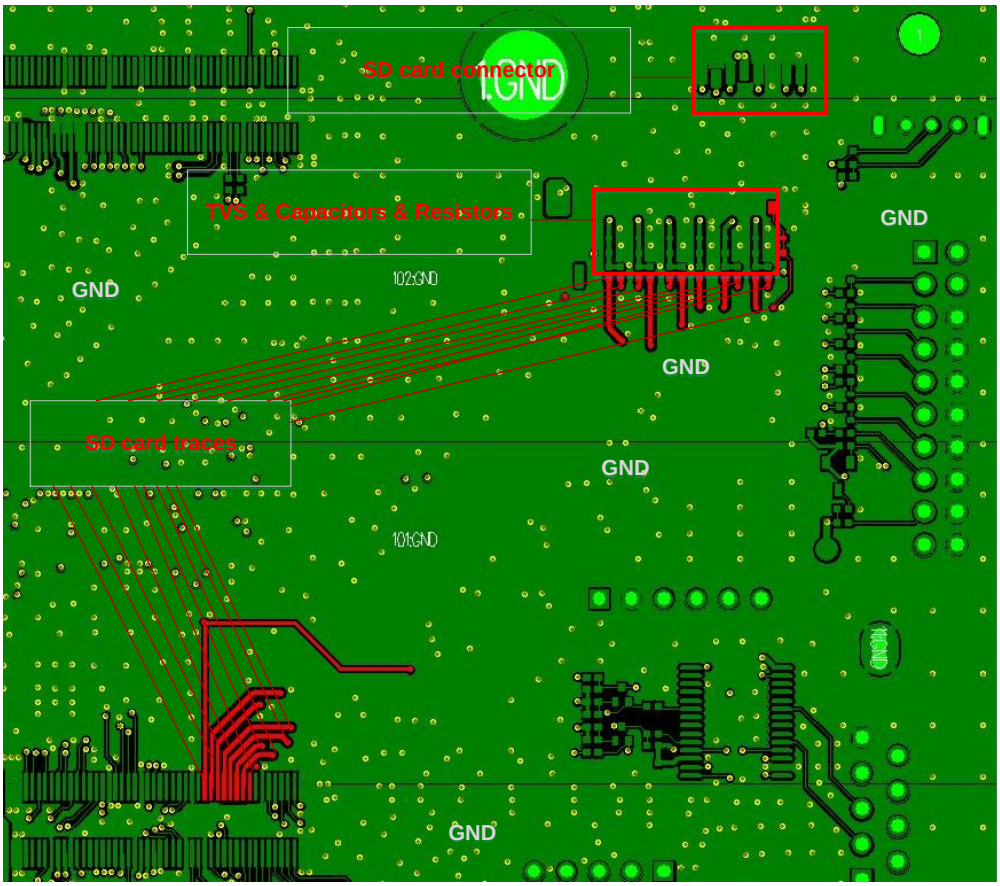

Figure 22: Overview of SD Card Signal Traces (EVB 1st Layer)

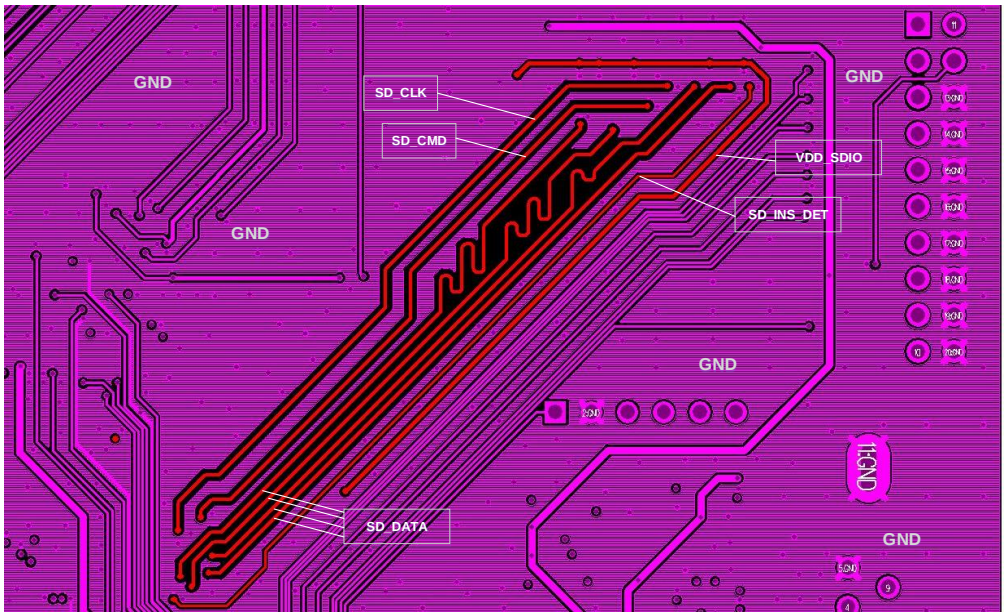

Figure 23: Overview of SD Card Signal Traces (EVB 3rd Layer)

3.7. WLAN Interface

- Keep SDIO signals far away from other sensitive circuits/signals such as RF circuits, analog signals, etc, as well as noisy signals such as clock and DC-DC signals, etc.
- The total length of each SDIO signal trace should be less than 23 mm, and the difference between them should be less than 1 mm.
- The load capacitance for SDIO signal traces should be less than 15 pF.
- Keep the impedance of SDIO signal traces at 50 Ω ±10 %, maintaining the integrity of the reference plane. SD_CLK and SD_CMD should be surrounded with ground on the layer and adjacent ground planes If limited by space, the SD_DATA0 to SD_DATA3 could be surrounded with ground together.

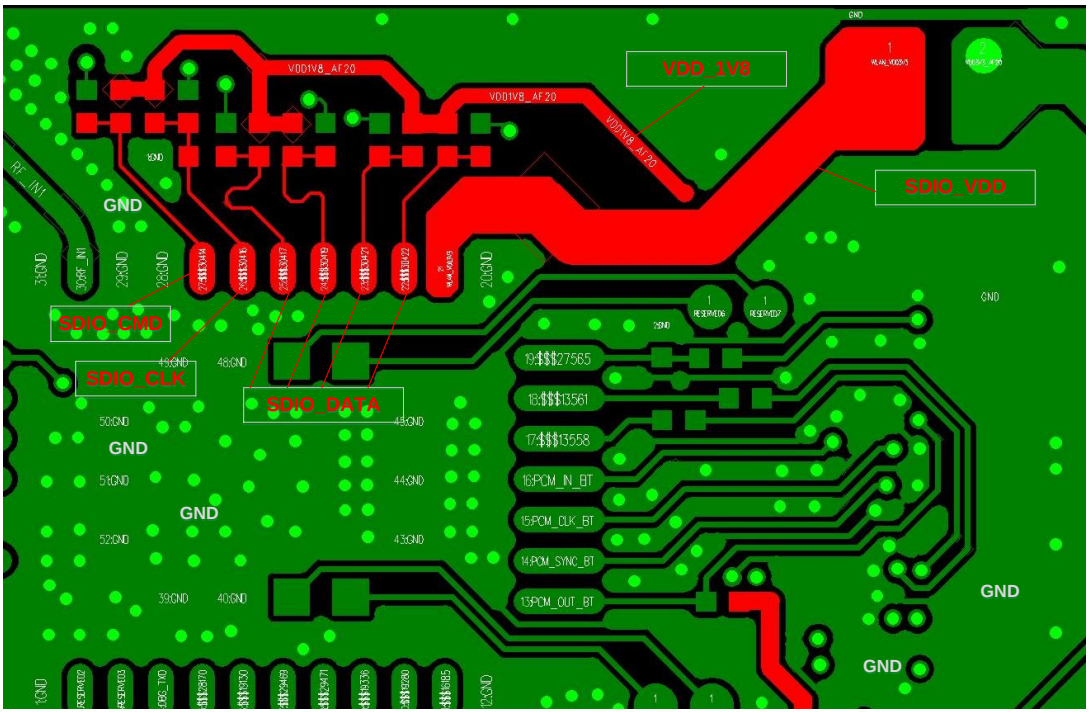

Figure 24: Overview of SDIO Signal Traces (FC20 TE-A 1st Layer)

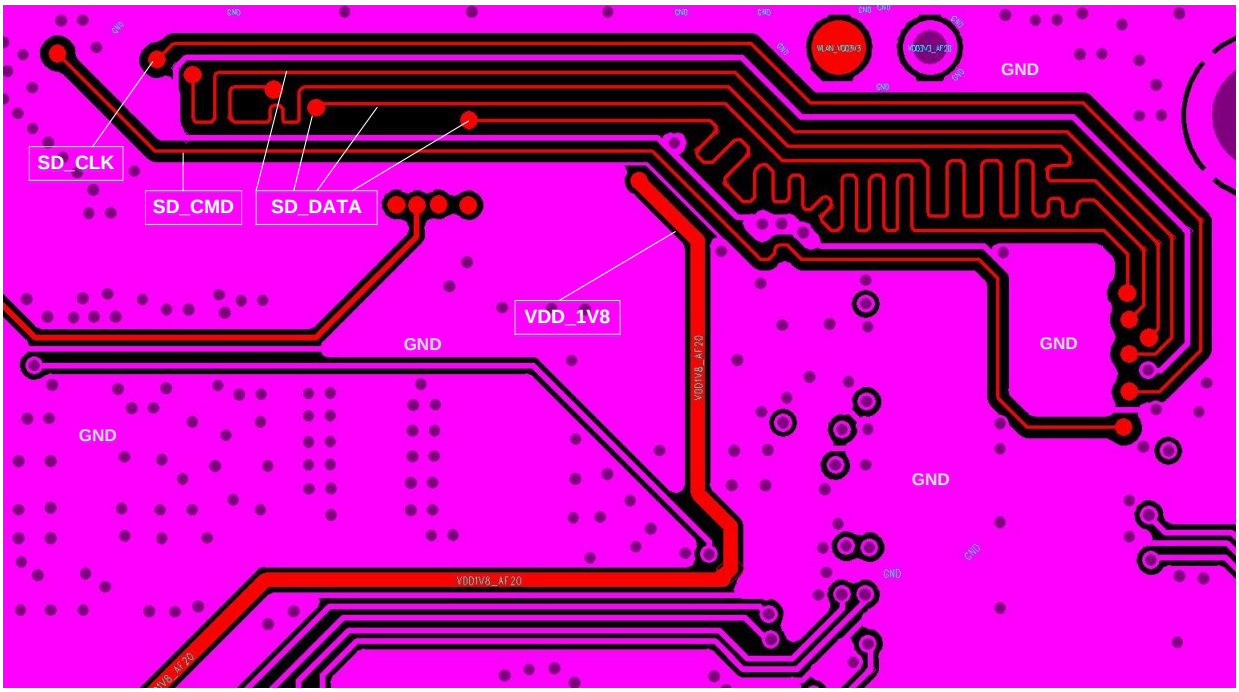

Figure 25: Overview of SDIO Signal Traces (FC20 TE-A 3rd Layer)

3.8. (U)SIM Interface

- The total length of each (U)SIM signal trace should be less than 200 mm.
- Isolate USIM_CLK and USIM_DAT with ground plane to avoid the interference between each other.
- The peripheral components such as TVS, capacitors and resistors should be put near the (U)SIM card connector.

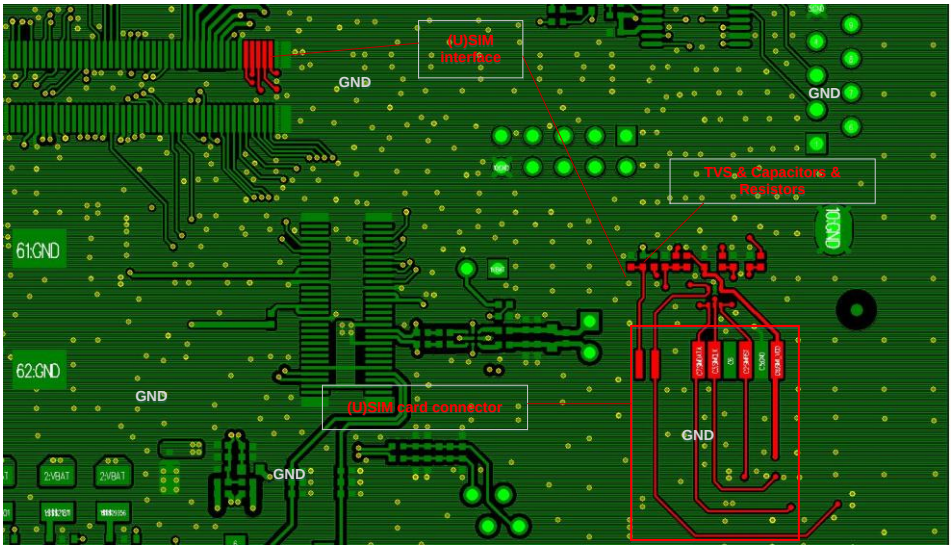

Figure 26: Overview of (U)SIM Signal Traces (EVB 1st Layer)

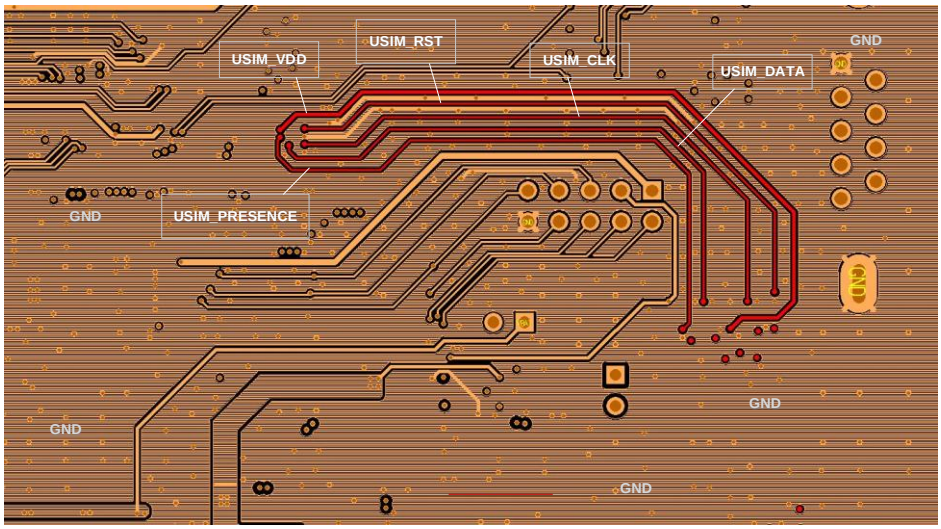

Figure 27: Overview of **(U)SIM Signal Traces (EVB 2nd Layer)**

3.9. ADC Interface

All ADC signal traces should be surrounded with ground.

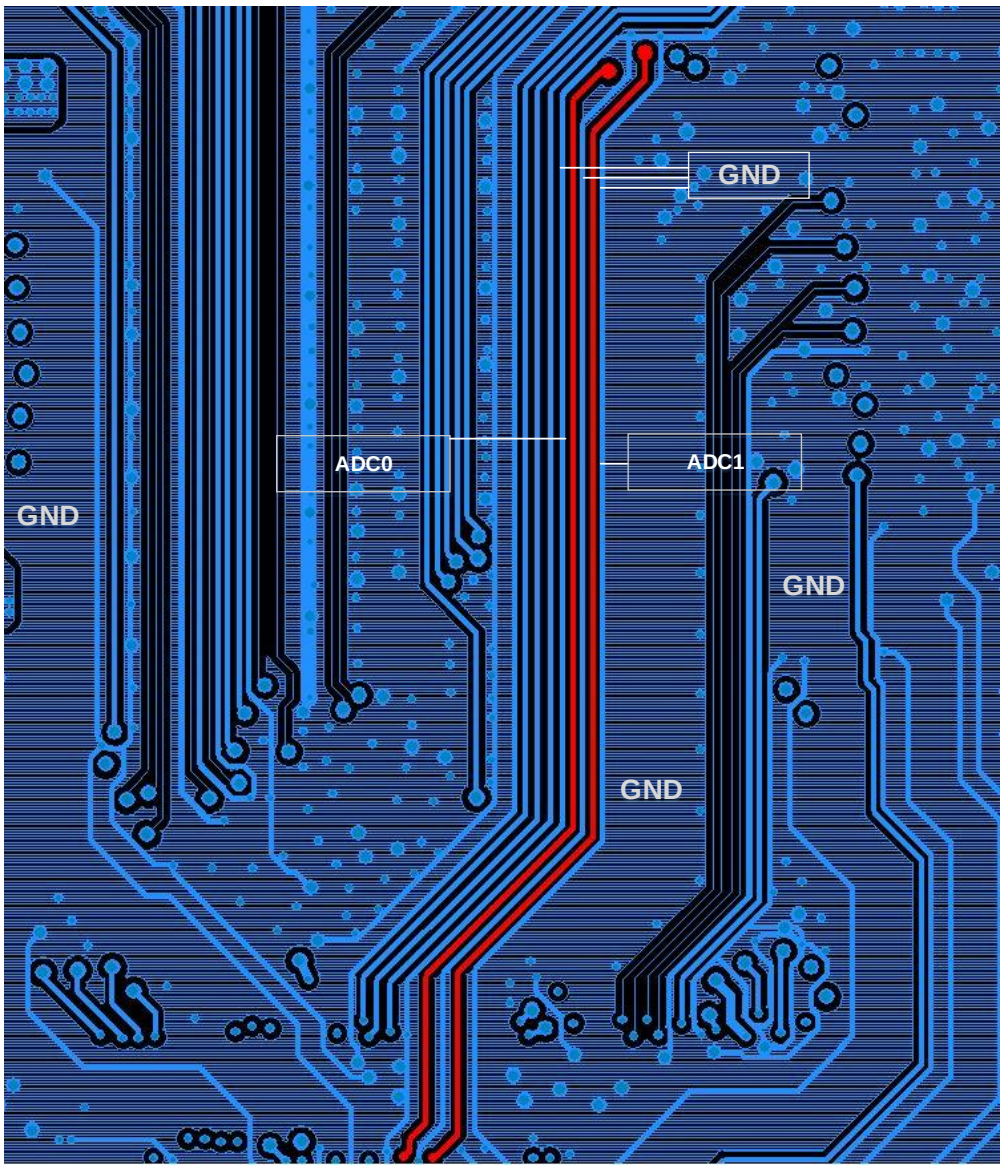

Figure 28: Overview of ADC Signal Traces (EVB 3rd Layer)

3.10. GPIOs

- Keep GPIO traces away from interference signals such as clock, RF and power supplies, etc.
- Filter capacitors need to be added and be placed close to the module when GPIO is used as input.

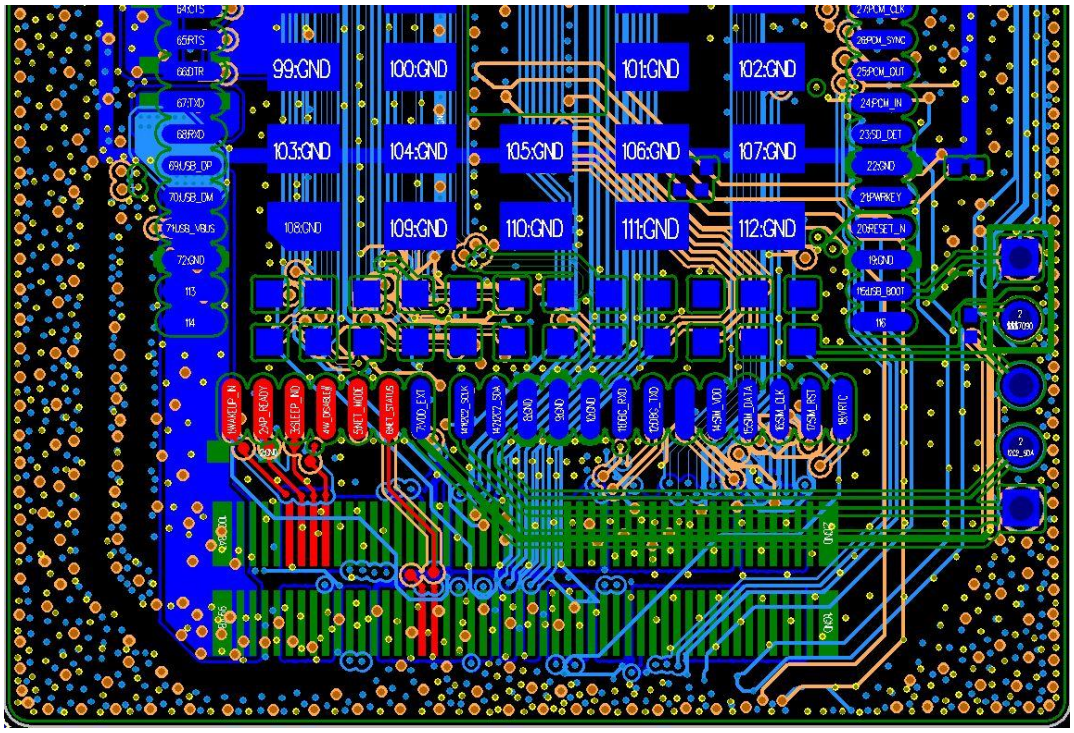

Figure 29: Overview of GPIO Signal Traces (TE-A without Copper Pouring)

3.11. Antenna Interfaces

3.11.1. PCB Structures of Microstrip And Coplanar Waveguide

3.11.1.1. PCB Structure of Microstrip Waveguide

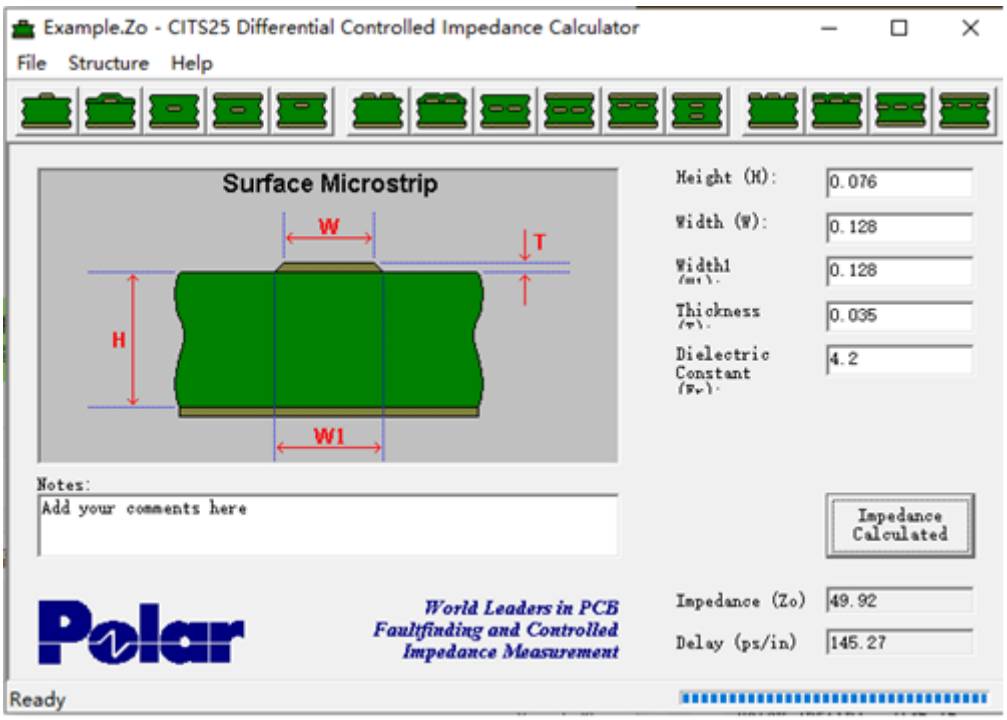

Figure 30: PCB Structure of Microstrip Waveguide

3.11.1.2. PCB Structure of Coplanar Waveguide

Factors affecting impedance include dielectric constant (usually 4.2–4.6, here 4.4), dielectric layer height (H), RF trace width (W), the spacing between RF traces and the ground (S) and copper thickness (T). When T = 0.035 mm, the following table lists the recommended values of W and S for 50 Ω coplanar waveguide under different PCB structures.

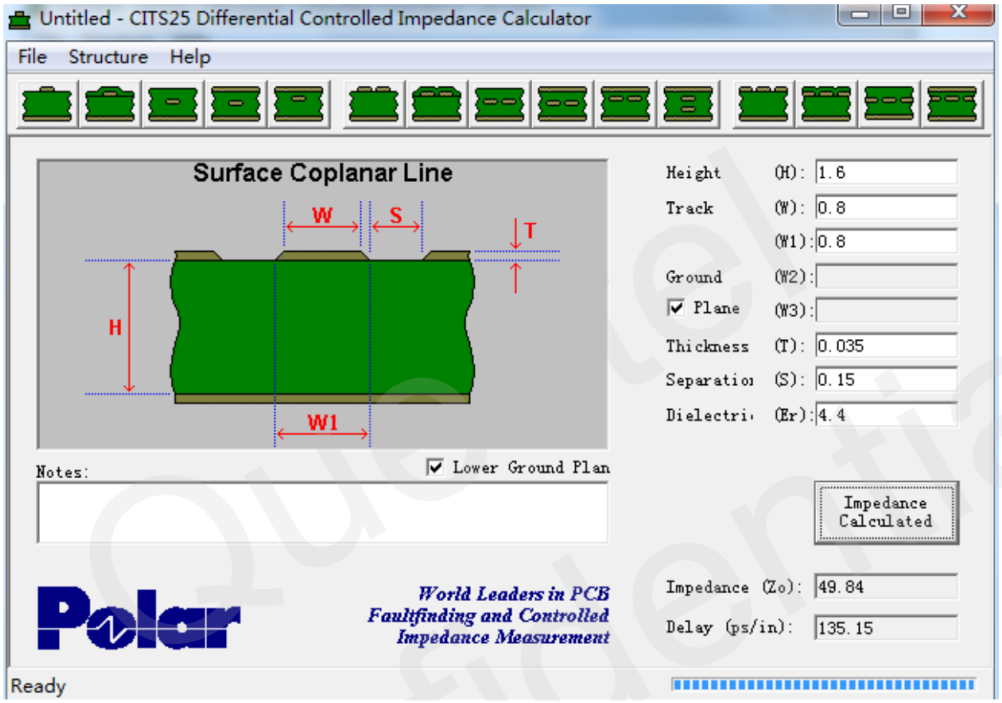

Figure 31: PCB Structure of Coplanar Waveguide

Table 2: Recommended Values of W and S for 50 Ω Coplanar Waveguide under Different PCB Structures

Dielectric Height (H)	RF Trace Width (W)	Spacing Between RF Trace and The Ground (S)
0.076 mm	0.1188	0.15 mm
0.1 mm	0.1623 mm	0.2 mm
0.15 mm	0.24 mm	0.2 mm
0.8 mm	0.8 mm	0.18 mm
1.0 mm	0.8 mm	0.17 mm
1.2 mm	0.8 mm	0.16 mm
1.6 mm	0.8 mm	0.15 mm
2 mm	0.8 mm	0.14 mm

3.11.2. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance.

If there is a 2-layer PCB, the top layer is used for signal trace routing, and the bottom layer should be the reference ground layer, as shown in ***Figure 32*** If there is a 4-layer PCB, the reference ground layer can be the second, the third, or the fourth layer. If the third layer is selected as the ground layer, the second layer should be kept out and the width should be at least 5 times the width of the trace，as shown in ***Figure 34***. The following are reference designs of microstrip and coplanar waveguide with different PCB structures.

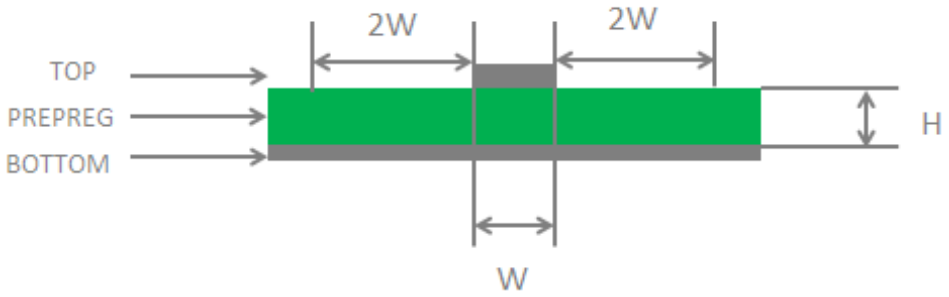

Figure 32: Microstrip Design on a 2-layer PCB

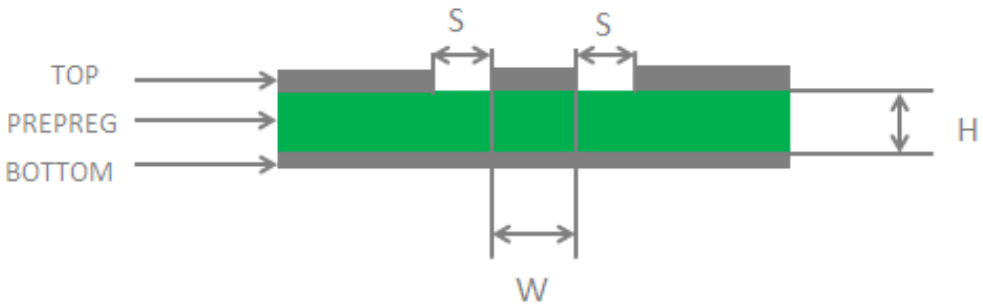

Figure 33: Coplanar Waveguide Design on a 2-layer PCB

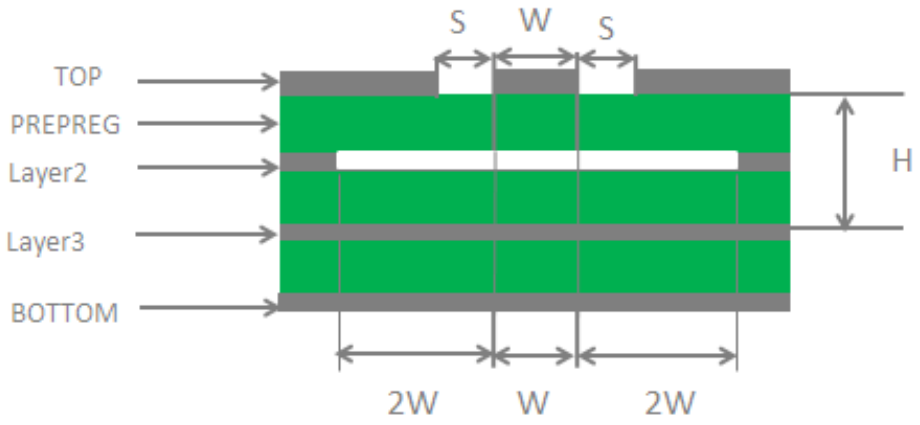

Figure 34: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

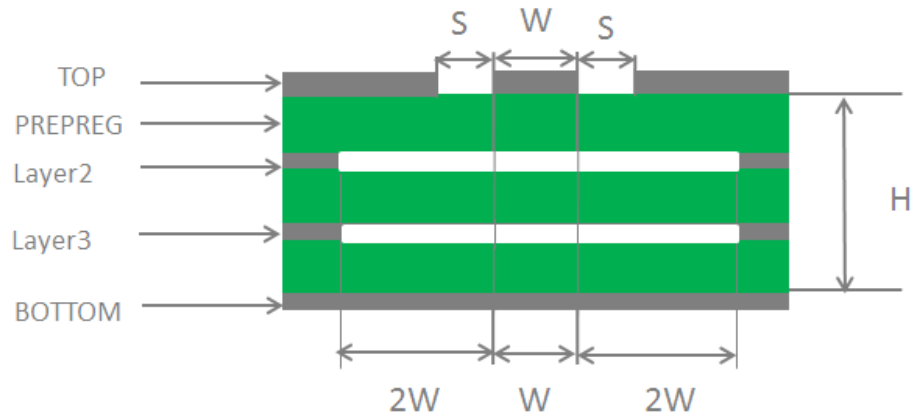

Figure 35: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

3.11.3. PCB Layout Considerations of Coplanar Waveguide

There are 6 guidelines of the PCB layout should be taken into consideration. Each guideline is corresponding to the marks in the following two figures respectively.

1. Control the trace width (W) and the spacing between RF traces and grounds (S) corresponding to the 50 Ω coplanar waveguide. Taking common PCB board with FR4 medium (dielectric constant 4.2) and copper thickness of 35 μm as an example, the W and S corresponding to the thickness between different signal layers and reference grounds are shown in ***Table 2***. It is particularly reminded that PCB manufacturers need to control the accuracy of the W and S.
2. Fully contact the GND pin pad next to the RF trace with ground plane and not design it as design thermal relief pad.

3. Leave a small keepout area for the RF traces on the top layer to reduce parasitic effects. Keep the traces as short as possible. Avoid right-angle routing for RF traces and 135 degrees is recommended when traces turn corner.
4. Keep a certain distance between signal pad and ground when packaging the component. If the signal pad is SMD type, pour the copper on the corresponding signal pad.
5. Make sure that reference ground planes corresponding to RF traces are complete. Increase the number of GND vias for current reflow of RF signal, and the spacing between GND vias and RF traces should be more than two times of trace width. Keep the ground plane area for RF traces within the same layer be as large as possible and the reference ground plane in the other layer complete as well. Besides, the number of through vias for those two ground planes should be sufficient.
6. The pads for PI type matching circuit consisting of a resistor and two capacitors should be near the module's antenna pins.

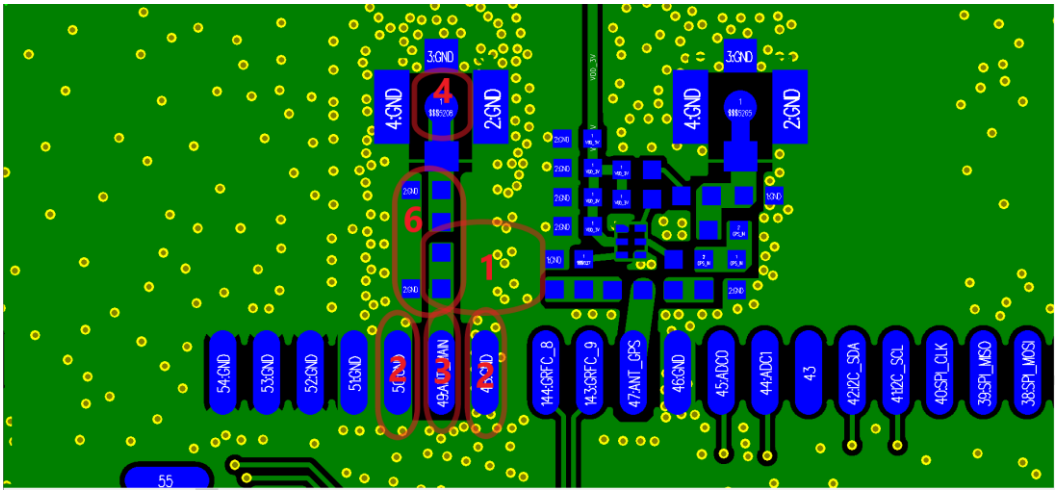

Figure 36: Overview of RF Traces (EVB 1st Layer)

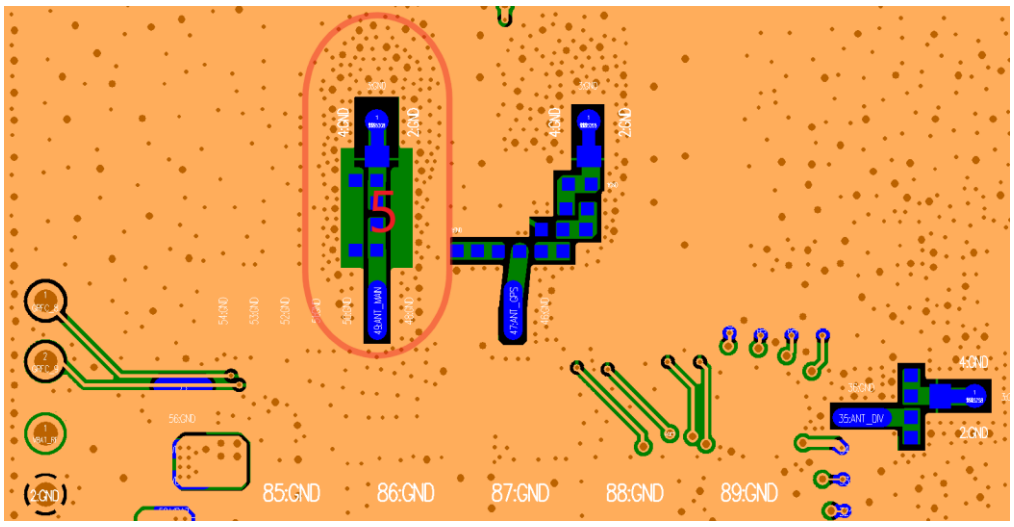

Figure 37: Overview of RF Traces (EVB 1st and 2nd Layers)

4 Thermal Design

For more details of the thermal design of the PCB, please refer to ***document [5]***.

5 Appendix A References

Table 3: Related Documents

SN	Document Name	Remark
[1]	Quectel_EC21_Footprint&Part	EC21 series Footprint&Part
[2]	Quectel_EC25_Footprint&Part	EC25 series Footprint&Part
[3]	Quectel_EC20_R2.1_Footprint&Part	EC20 R2.1 Footprint&Part
[4]	Quectel_EG25-G&EG21-G_Footprint&Part	EG25-G&EG21-G Footprint&Part
[5]	Quectel_LTE_Module_Thermal_Design_Guide	Thermal design guide for LTE standard, LTE-A and Automotive modules

Table 4: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
ESD	Electrostatic Discharge
GPIO	General-Purpose Input/Output
I/O	Input/Output
LTE	Long Term Evolution
PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PHY	Physical Layer
RF	Radio Frequency
SD	Secure Digital

SGMII	Serial Gigabit Media Independent Interface
USB	Universal Serial Bus
(U)SIM	(Universal) Subscriber Identity Module
VBAT	Voltage at Battery
WLAN	Wireless Local Area Network