

APPLICATION NOTE FOR CTPM_CHIPSEMI V1.0.1--2023-12-08

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1. I2C Communication

1.1 I²C timing sequence

The CHSC6xxx supports standard I²C interface, and acts as slave.

I²C Master can read any internal register and RAM space of the CHSC6xxx via I²C.

The recommended communication speed is 100-400Kbps.

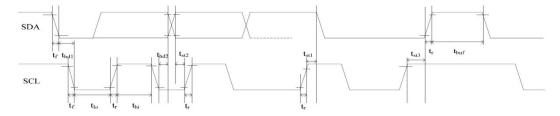


Figure 1. I²C timing sequence

Table 1. I²C timing parameter

parameter	symbol	MIN	MAX	unit
SCL low period	tlo	1.3		us
SCL high period	thi	0.6		us
SCL setup time for START condition	tst1	0.6		us
SCL setup time for STOP condition	tst3	0.6		us
SCL hold time for START condition	thd1	0.6		us
SDA setup time	tst2	0.1		us
SDA hold time	thd2	0		us
Rise time	tr		300	ns
Fall time	tf		300	ns
I2C bus free time between Stop and Start	tbuf	1.3		us



1.2 IIC communication read and write process

Device address: The 7-bit address is **0x2E**. After moving 1 bit to the left, the write communication is **0x5C** and the read communication is **0x5D**.

IIC communication write process:

Start + 0x5C + ACK + ADDR[15:8] + ACK + ADDR[7:0] + ACK + DATA

+ ACK + ... + DATA + ACK + STOP

S	id	w	Α	Addr[15:8]	Α	Addr[7:0]	Α	Data[7:0]	Α	 Data[7:0]	Α	S
Т			С		С		С		С		С	Т
Α			K		K		K		K		K	0
R												Р
Т												

IIC communication reading process:

Step1: Start + 0x5C + ACK + ADDR[15:8] + ACK + ADDR[7:0] +

ACK + STOP

Step2: Start + 0x5D + ACK + DATA + ACK + ... + DATA + NAC K + STOP

S	S	id	w	Α	Addr[15:8]	Α	Addr[7:0]	Α	S
Т	Т			С		С		С	Т
Е	Α			K		K		K	0
Р	R								Р
1	Т								

S	s	id	r	Α	Data[7:0]	Α	Data[7:0]	Α	 N	S
Т	Т			С		С		C	Α	т
Е	Α			K		K		K	С	0
Р	R								K	Р
2	Т									

Example: HOST responds to interrupt and reads the waveform of touch coordinate data.

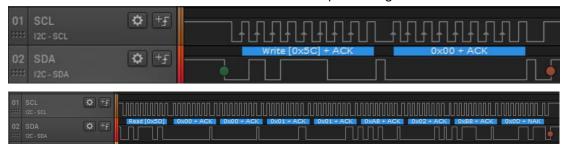
The INT pin of CHSC6XXX triggers an interrupt and HOST reads coordinate data once.







Write device address 0x5C and write 0x00 register addresses Write device address 0x5D to read touch data of required length



1.3 Format of touch data

Format of touch data reported by CHSC6xxx to HOST.

Address	BIT7	BIT6	BIT5	BIT4	BIT3	BIT2	BIT1	BIT0
0x00	Reserve	Reserved: default 0						
0x01	Reserve	d: default (0					
0x02	The num	ber of tou	ch points					
0x03	point 1:	touch ever	nt		point 1:	X coordin	nate [11:8]	
	Put dow	n : 0				(X, Y)		
	contact	:8				///		
	Put up :4	1						
0x04	point 1:	X coordina	te [7:0]					
0x05	point 1:	Touch ID			point 1:	Y coordir	nate [11:8]	
0x06	point 1:	Y coordina	te [7:0]					
0x07	point 1:7	ouch pres	sure (Res	erved)				
0x08	point 1:7	ouch area	(Reserve	d)				
0x09	point 2:	touch ever	nt		point 2:	X coordir	nate [11:8]	
	Put dow	n : 0						
	contact	8						
	Put up :4							
0x10	point 2:	X coordina	te [7:0]					
0x11	point 2:	Touch ID			point 2:	Y coordin	nate [11:8]	
0x12	point 2:	Y coordina	te [7:0]					
0x13	point 2:1	point 2:Touch pressure (Reserved)						
0x14	point 2:1	point 2:Touch area (Reserved)						

2. The way the IIC master accesses the touch IC memory

2.1 Direct Address Access (DMA mode)

Direct address access mode, which means that the IIC master can access any address of the chsc6xxx through a 16-bit address. Firmware upgrade, obtaining TP information, etc. must work in this mode.

2.2 Mapping access mode (Mapping mode)



Read and write accesses to TP are mapped to a fixed memory space, and the FW can configure the mapped memory space mentioned here (defined as MTK_TXRX_BUF, and set the address to 0x809000). The maximum mapped space size for chsc6xxx read and write operations is 128 bytes. In this mode, the data written on the IIC in addition to the SLAVE address are written as ordinary data to the configured RAM space, when reading operation, the data on the IIC is the data in the configured RAM space, read coordinates are working in this mode.

The mapped address access mode is set to prevent the HOST from inadvertently writing incorrect data to the chsc6xx's internal registers, which may cause the IC to fail to run the firmware or unexpected unknown errors

2.3 Switching between two address access modes

By default, chsc6xxx works in the "direct address access mode", and the firmware will switch to the "mapped address access mode" by modifying the register after running, that is, the normal working mode is "mapped address access mode". The driver only needs to call the tlsc6x_tpd_reset() function to switch the direct address mode to the mapping address.

When the driver needs to obtain some information of chsc6xxx, such as the firmware version of TP, Vendor ID and Project ID, etc., it is necessary to switch the mapped address access mode to the direct address access mode, and then directly read the corresponding memory area and decode it;

The function interface for the driver to switch the mapped address mode to the direct address access mode is:

int tlsc6x_set_dd_mode(void)

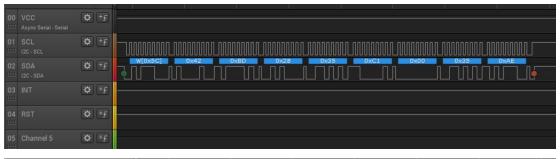
3. Register operation

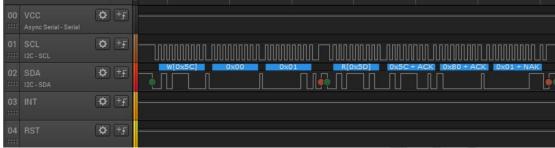
3.1 Get TP related information

In the first step,reset TP once, and after a delay of 30ms, the HOST write 0x42 0xBD 0x28 0x35 0xC1 0x00 0x35 0xAE switches TP to direct address access mode (DMA). Wait 20ms to check whether the direct address switchover is successful. If the IIC address can be obtained from address 0x0001, it indicates success, as shown in the following figure:

Address	Bit address	Variable Name	Description
0x42BD	15:0	1	Write 0x28 0x35 0xc1
			0x00 0x35 0xae to
			enter DMA mode







3.1.1 VID PID CFG

Address	Bit address	Variable Name	Description
0x9e00	31: 0	tlsc_vendor_id	Read out Vendor ID
		tlsc_project_id	Project ID Configure
		tlsc_cfg_version	firmware version from
			TP



1st Short Type data 0x0E3E: [8:0]-Project ID[8:0], [15:9]-vendor ID[6:0];

2st Short Type data 0x100E: [5:4]-Project ID[10:9], [7:6]-vendor ID[8:7],

[15:10]-configure firmware version

Decode:

Vendor ID = 0x7;

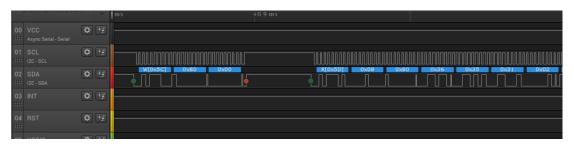
Project ID = 0x3E;

configure firmware version = 0x4;

3.1.2 Boot firmware version

Address	Bit address	Variable Name	Description
0x8004	15:0	tlsc_boot_version	Read boot firmware
			version

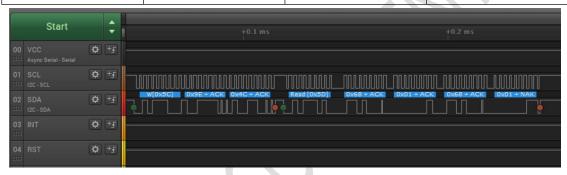




Boot firmware version:0x231

3.1.3 Resolution

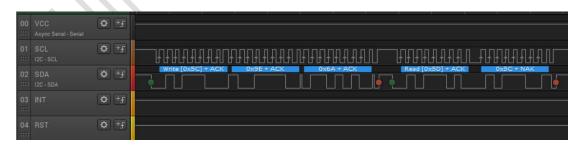
Address	Bit address	Variable Name	Description
0x9e4c	15:0	1	Read out X-direction
			resolution
0x9e4e	15:0	1	Read out Y-direction
			resolution



X-direction resolution:0x168 Y-direction resolution:0x168

3.1.4 IIC Address

Address	Bit address	Variable Name	Description
0x9e6a	7:0	1	Read out i2c slave
			address from TP



3.1.5 Chip Type

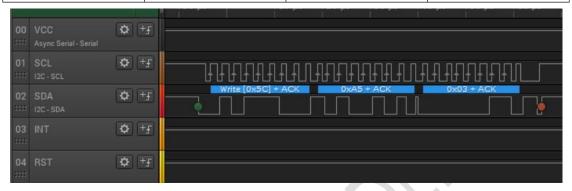
Address	Bit address	Variable Name	Description
0x9e6b	4:0	g_tlsc6x_chip_code	Read out Chip Type
			from TP



After the read operation is complete, reset TP to exit the direct address mode or write 0x5 at address 0x03 to switch back to the mapped address mode.

The following operations are performed in mapped address mode 3.2 Enter sleep mode

Address	Bit address	Variable Name	Description
0xA5	7:0	1	Write 0x03 to enter
			sleep mode



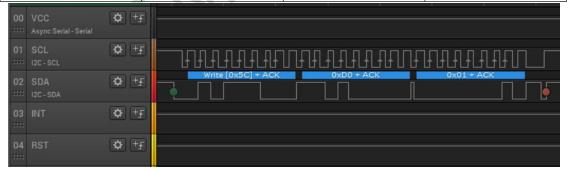
Exit sleep mode after reset TP once

The function interface for the driver:

int tlsc6x_do_suspend(void)
void tlsc6x_resume_work()

3.3 Enter Gesture mode

Address	Bit address	Variable Name	Description
0xD0	7:0	1	Write 0x01 to enter
			gesture mode
			Write 0x00 exit



Exit gesture mode after reset TP once (equal to write 0x00)

Gesture ID

Address	Bit address	Variable Name	Description
0xd3	7:0	gestrue_id	0x20 GESTRUE_LEFT
			0X21 GESTRUE_RIGHT
			0X22 GESTRUE_UP
			0X23 GESTRUE_DOWN
			0X24 GESTRUE_DOUBLECLICK



0X30 GESTRUE_O
0X31 GESTRUE_W
0X32 GESTRUE_M
0X33 GESTRUE_E
0X34 GESTRUE_C
0X46 GESTRUE_S
0X54 GESTRUE_V
0X65 GESTRUE_Z
0X44 GESTRUE_L