Product Specification

Part Name: OEL Display Module
Customer Part ID:
Part ID:QG-6432TSWEG02
Ver: A

Customer:
Approved by

From: ³É¶¼Àû»ÝÀûÌØ×Ô¶¯»¯¿Æ¼¼ÓÐÏÞ¹«Ë¾
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Revised History

Part Number	Revision	Revision Content	Revised on
QG6432TSWEG02	A	New	20140626

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1. Basic Specifications

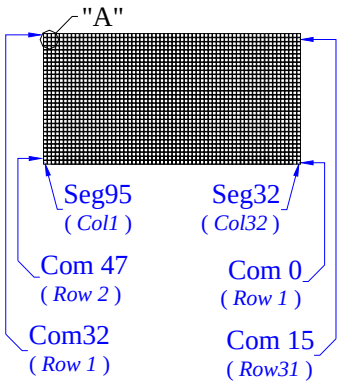
1.1 Display Specifications

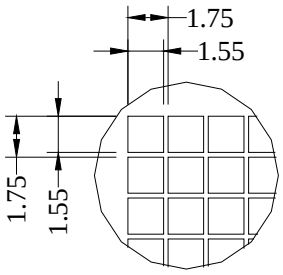
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (White)
3) Drive Duty: 1/32 Duty

1.2 Mechanical Specifications

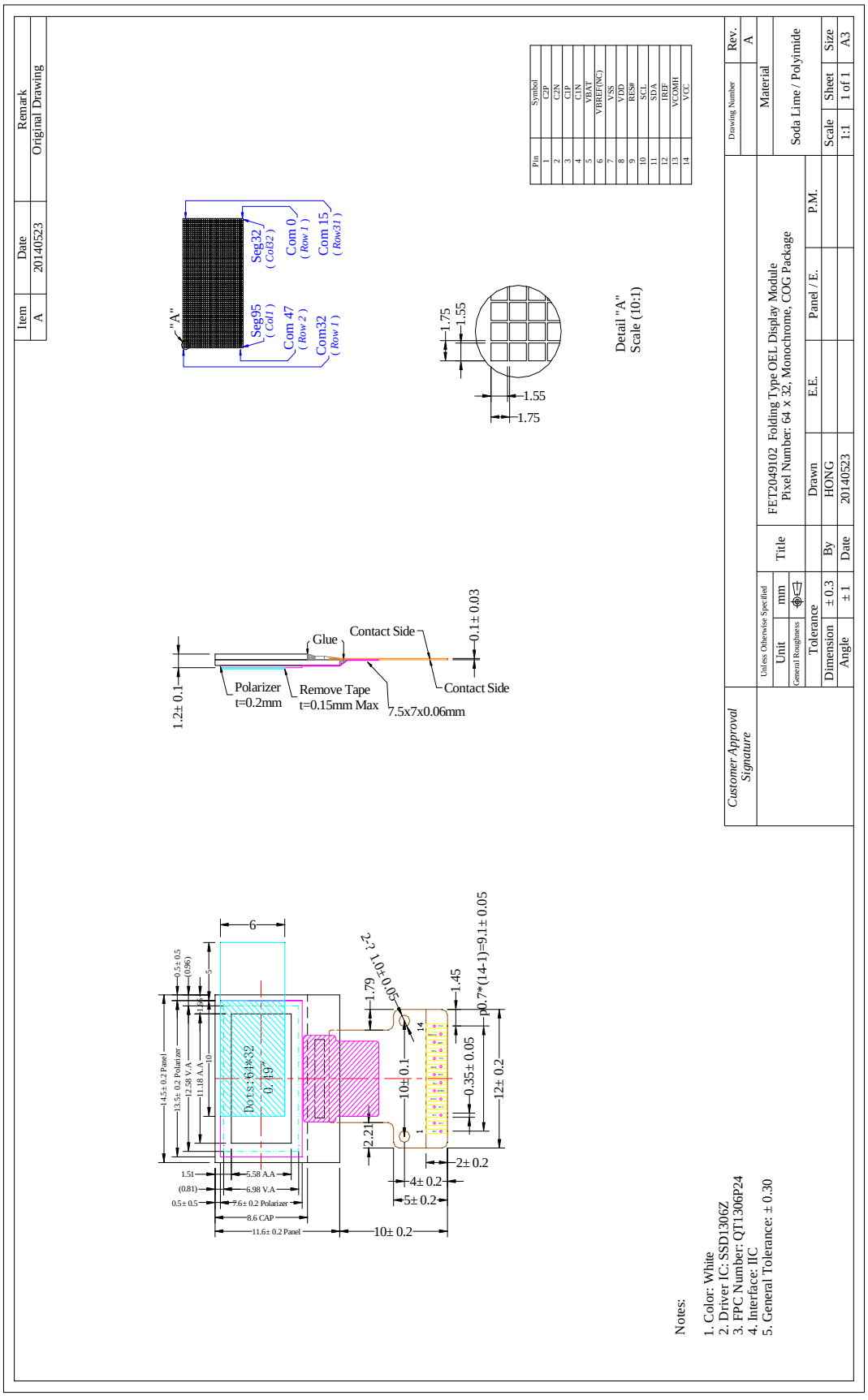
1) Outline Drawing: According to the annexed outline drawing
2) Number of Pixels: 64 × 32
3) Panel Size: 14.5 × 11.6 × 1.2 (mm)
4) Active Area: 11.18 × 5.58 (mm)
5) Pixel Pitch: 0.175 × 0.175 (mm)
6) Pixel Size: 0.155 × 0.155 (mm)
7) Weight: TBD

1.3 Active Area / Memory Mapping & Pixel Construction





1.4 Mechanical Drawing



1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
8	VDD	P	**Power Supply for Logic** This is a voltage supply pin. It must be connected to external source.
7	VSS	P	**Ground of Logic Circuit** This is a ground pin. It acts as a reference for the logic pins. It must be connected to external ground.
14	VCC	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A stabilization capacitor should be connected between this pin and V_{SS} when the converter is used. It must be connected to external source when the converter is not used.
Driver			
12	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and V_{SS}. Set the current at 12.5μA maximum.
13	VCOMH	O	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and V_{SS}.
DC/DC Converter			
5	VBAT	P	**Power Supply for DC/DC Converter Circuit** This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be connected to V_{DD} when the converter is not used.
3 / 4 1 / 2	C1P / C1N C2P / C2N	I	**Positive Terminal of the Flying Inverting Capacitor** **Negative Terminal of the Flying Boost Capacitor** The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
Interface			
9	RES#	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
10	SCL	I	**IIC Bus Clock Signal** The transmission if information in the I2C bus is following a clock sigmal. Each transmission of data bit is taken place during a single clock period of this pin.
11	SDA	I/O	**I2C Bus Data Signal** This pin acts as a communication channel between the transmitter and the receiver.
Reserve			
6	VBREF	-	NC

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD}	-0.3	4	V	1, 2
Supply Voltage for Display	V_{CC}	0	16	V	1, 2
Supply Voltage for DC/DC (Internal DC/DC Enable)	*V_{bat}*	*-0.3*	*4.3*	*V*	*1, 2*
Operating Temperature	T_{OP}	-40	85	°C	
Storage Temperature	T_{STG}	-40	85	°C	3
Life Time (120 cd/m^2)		10,000	-	hour	4
Life Time (80 cd/m^2)		30,000	-	hour	4
Life Time (60 cd/m^2)		50,000	-	hour	4

Note 1: All the above voltages are on the basis of "V_{SS} = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Optics & Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{CC} = 7.25V, T_a = 25°C, 50% Checkerboard.
Software configuration follows Section 4.4 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (V_{CC} Supplied Externally)	L_{br}	Note 5	160	-	-	cd/m^2
Brightness (V_{CC} Generated by Internal DC/DC)	*L_{br}*	*Note 6*	*160*	*180*	-	*cd/m^2*
C.I.E. (White)	(x) (y)	C.I.E. 1931	0.28 0.31	0.32 0.35	0.36 0.39	
Dark Room Contrast	CR		-	2000:1	-	
Viewing Angle			-	Free	-	degree

* Optical measurement taken at V_{DD} = 2.8V, V_{CC} = 7.25V.
Software configuration follows Section 4.4 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD}		1.65	2.8	3.3	V
Supply Voltage for Display (Supplied Externally)	V_{CC}	Note 5 (Internal DC/DC Disable)	7	-	9.0	V
Supply Voltage for DC/DC	*V_{BAT}*	*Internal DC/DC Enable*	*3.5*	*-*	*4.2*	*V*
Supply Voltage for Display (Generated by Internal DC/DC)	*V_{CC}*	*Note 6 (Internal DC/DC Enable)*	7	7.25	7.5	*V*
High Level Input	V_{IH}	I_{OUT} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{OUT} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{OUT} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V
Operating Current for V_{DD}	I_{DD}		-	180	300	μA
Operating Current for V_{CC} (V_{CC} Supplied Externally)	I_{CC}	Note 7	-	5	10	mA
Operating Current for V_{BAT} (V_{CC} Generated by Internal DC/DC)	*I_{BAT}*	*Note 8*	-	*10*	*15*	*mA*
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	5	μA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	2	10	μA

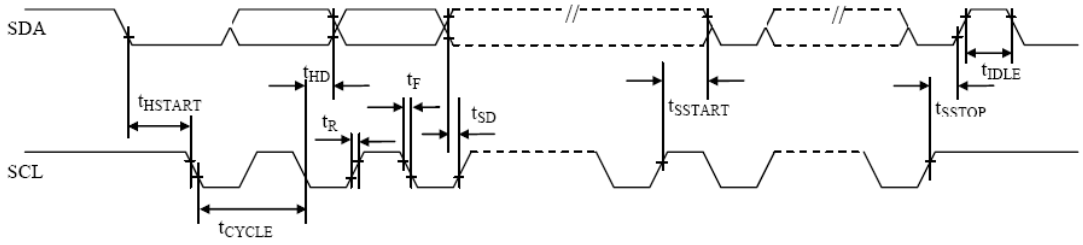
Note 5 & *6*: Brightness (L_{br}) and Supply Voltage for Display (V_{CC}) are subject to the change of the panel characteristics and the customer's request.
Note 7: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.
Note 8: V_{DD} = 2.8V, V_{CC} = 7.25V, 100% Display Area Turn on.
* Software configuration follows Section 4.4 Initialization.

3.3 AC Characteristics

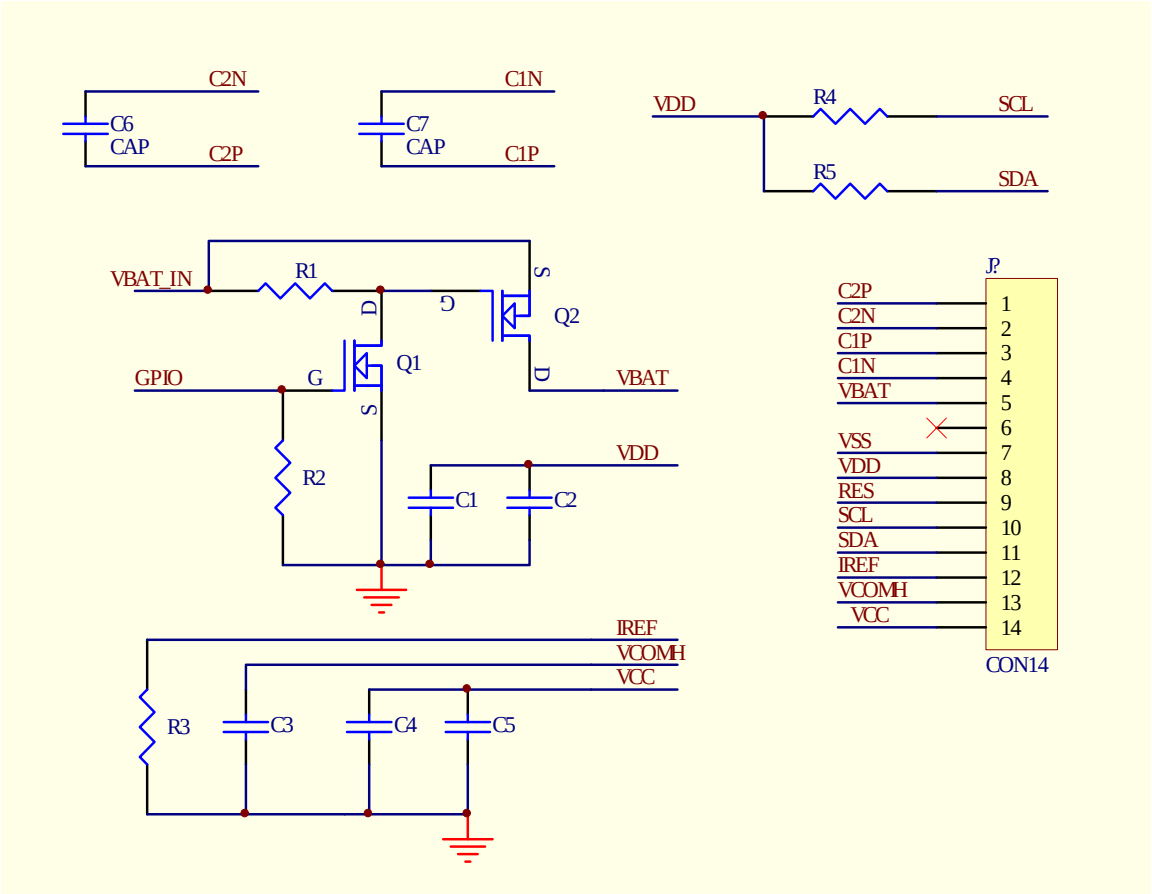
3.3. 1 I^2C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	μs
t_{HSTART}	Start Condition Hold Time	0.6	-	μs
t_{HD}	Data Hold Time (for "SDA_{OUT}" Pin)	0	-	ns
	Data Hold Time (for "SDA_{IN}" Pin)	300		
t_{SD}	Data Setup Time	100	-	ns
t_{SSTART}	Start Condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	μs
t_{SSTOP}	Stop Condition Setup Time	0.6	-	μs
t_R	Rise Time for Data and Clock Pin		300	ns
t_F	Fall Time for Data and Clock Pin		300	ns
t_{IDLE}	Idle Time before a New Transmission can Start	1.3	-	μs

* (V_{DD} - V_{SS} = 1.65V to 3.3V, T_a = 25°C)



3.3.2 I²C Interface with Internal Charge Pump



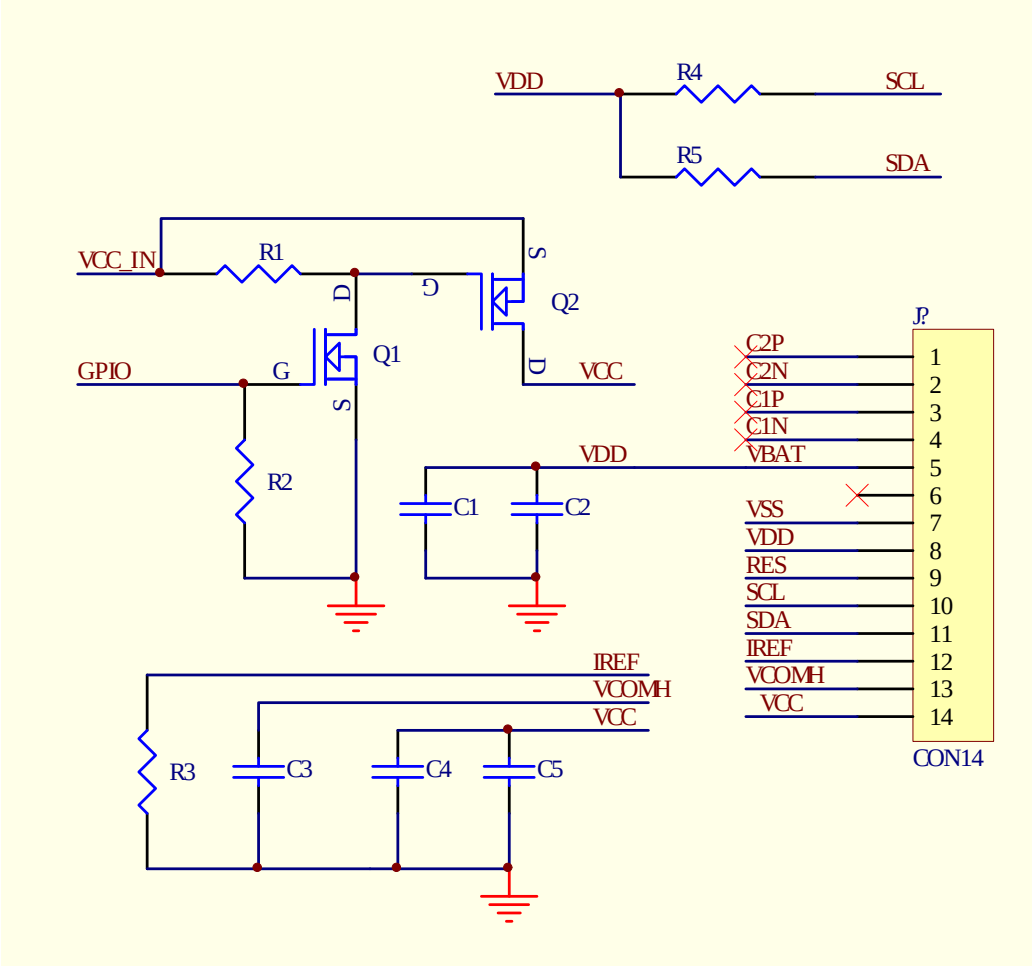
Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
C6,C7:	1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
R4, R5:	4. 7kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.3V, it should be equal to MPU I/O voltage.
VBAT_in:	3.5~4.2V

3.3.3 I²C Interface with External VCC



Recommended Components:

C1,:	0.1μF / 6.3V, X5R
C2:	4.7μF / 6.3V, X5R
C3:	2.2μF/ 16V, X7R
C4:	4.7μF / 16V, X7R
C5:	0.1μF / 16V, X7R
R3:	560KΩ, R3 = (Voltage at IREF - VSS) / IREF
R2, R1:	47kΩ
R4, R5:	4. 7kΩ
Q1:	FDN338P
Q2:	FDN335N

Notes:

VDD:	1.65~3.3V, it should be equal to MPU I/O voltage.
VCC_in:	7~7.5V

4.Functional Specification

4.1 Commands

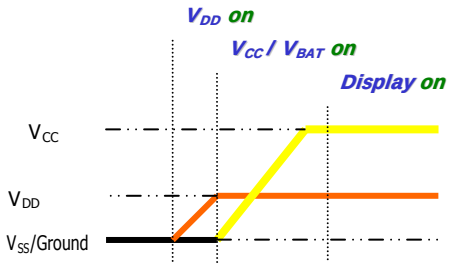
Refer to the Technical Manual for the SSD1306

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

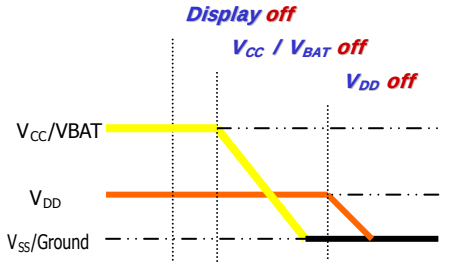
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{CC}/ V_{BAT}
6. Delay 100ms
   (When V_{CC} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC} / V_{BAT}
3. Delay 100ms
   (When V_{CC} / V_{BAT} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



Note 13:

1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} inside the driver IC, V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF.
2) V_{CC} / V_{BAT} should be kept float (disable) when it is OFF.
3) Power Pins (V_{DD}, V_{CC}, V_{BAT}) can never be pulled to ground under any circumstance.
4) V_{DD} should not be power down before V_{CC} / V_{BAT} power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

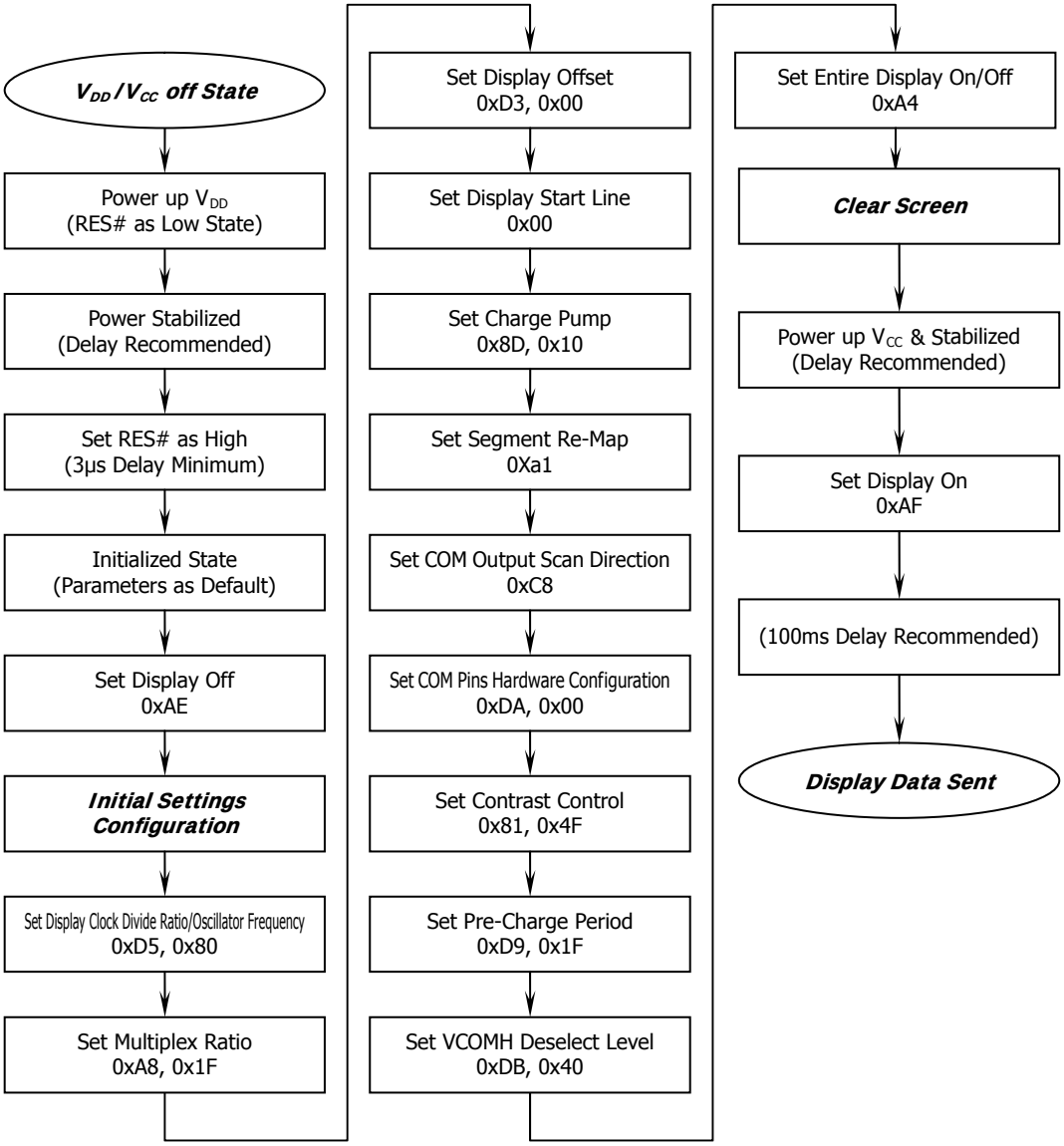
1. Display is OFF
2. 128×64 Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Contrast control register is set at 7Fh
9. Normal display mode (Equivalent to A4h command)

4.4 Actual Application Example

Command usage and explanation of an actual example

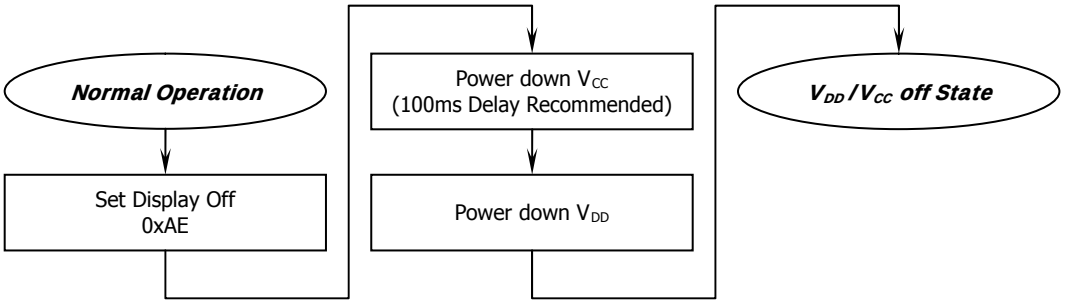
4.4.1 V_{CC} Supplied Externally

<Power up Sequence>

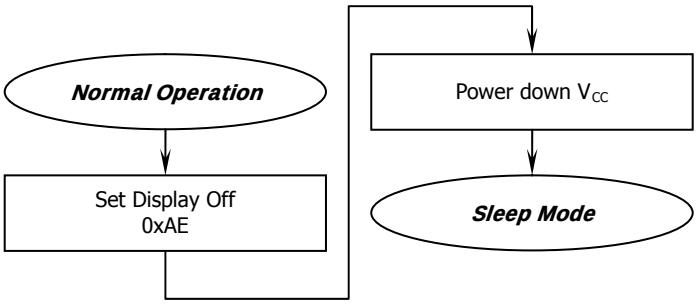


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

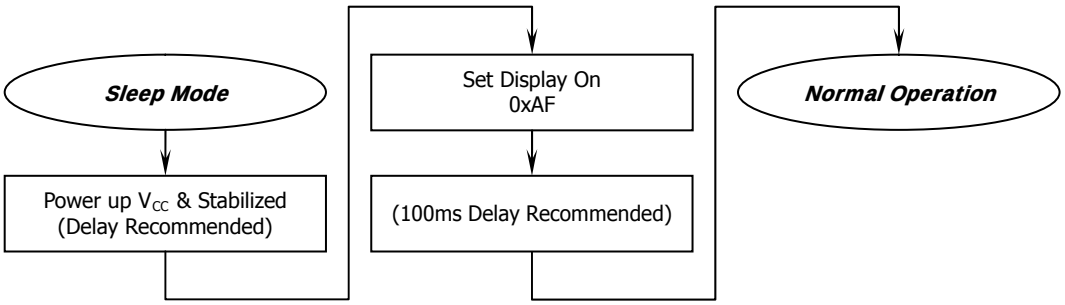
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



External setting

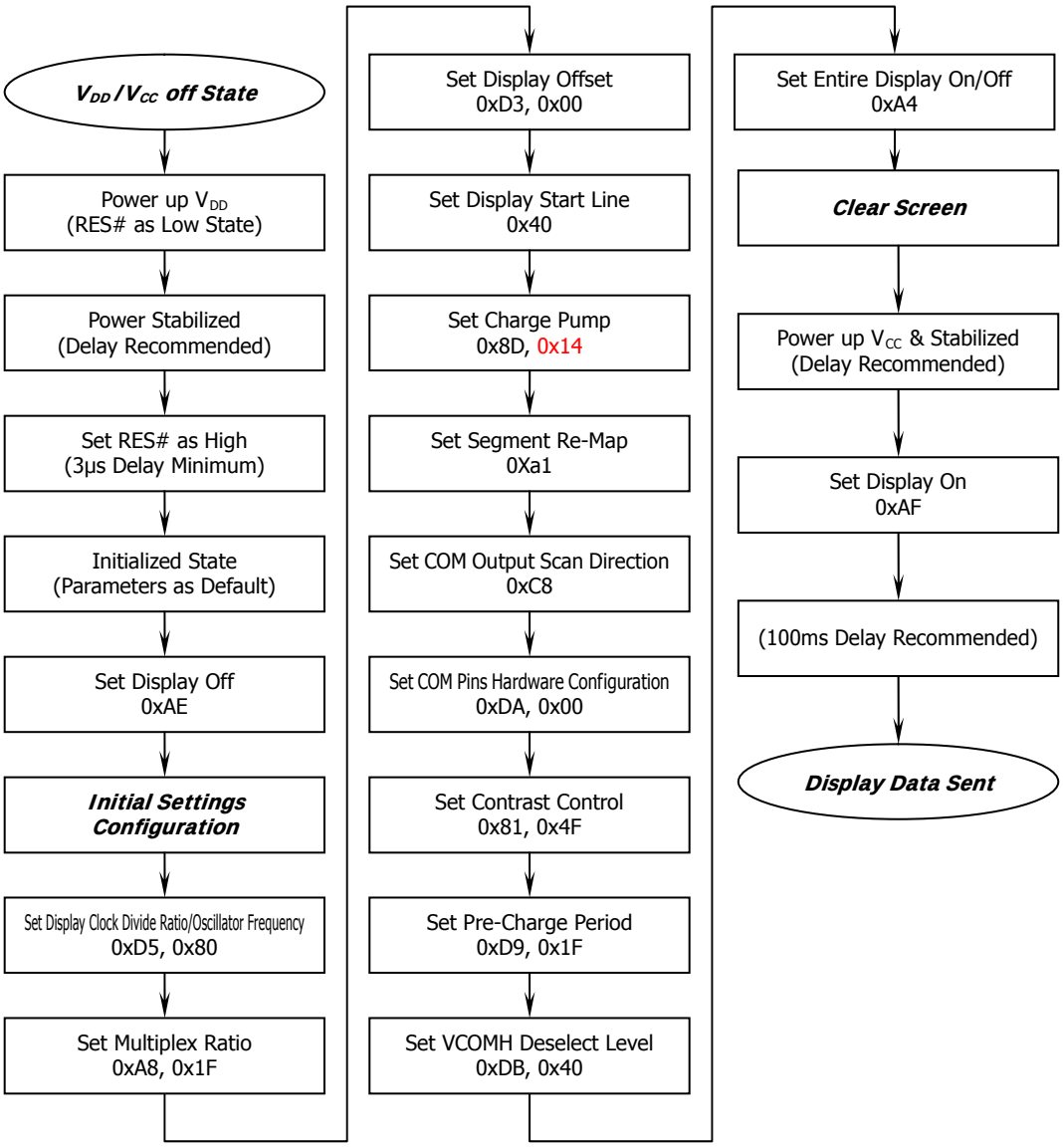
```
void SSD1306()
{
    RES=0;
    delay(1000);
    RES=1;
    delay(1000);

      write_i(0xAE);      /*display off*/

      write_i(0x00);      /*set lower column address*/
      write_i(0x12);      /*set higher column address*/

      write_i(0x00);      /*set display start line*/

      write_i(0xB0);      /*set page address*/
```

```
        write_i(0x81);      /*contract control*/
        write_i(0x4f);      /*128*/

        write_i(0xA1);      /*set segment remap*/

        write_i(0xA6);      /*normal / reverse*/

        write_i(0xA8);      /*multiplex ratio*/
        write_i(0x1F);      /*duty = 1/32*/

        write_i(0xC8);      /*Com scan direction*/

        write_i(0xD3);      /*set display offset*/
        write_i(0x00);

        write_i(0xD5);      /*set osc division*/
        write_i(0x80);

        write_i(0xD9);      /*set pre-charge period*/
        write_i(0x1f);

        write_i(0xDA);      /*set COM pins*/
        write_i(0x12);

        write_i(0xdb);      /*set vcomh*/
        write_i(0x40);

        write_i(0x8d);      /*set charge pump enable*/
        write_i(0x10);

        write_i(0xAF);      /*display ON*/
 }
void write_w(unsigned char dat)
{
    unsigned char m,da;
    unsigned char j;
    da=dat;
    for(j=0;j<8;j++)
    {
      m=da;
      SCL=0;
      m=m&0x80;
      if(m==0x80)
         {
           SDA=1;
         }
      else
         {
```

```
            SDA=0;
          }
       da=da<<1;
       SCL=1;
      }
      SCL=0;
      SCL=1;
}

void write_i(unsigned char ins)
{    start();
    write_w(0x78);
    write_w(0x00);
    write_w(ins);
    stop();
}
void write_d(unsigned char dat)
{
    start();
    write_w(0x78);
    write_w(0x40);
    write_w(dat);
    stop();
}

 void   start()
{
  SCL=1;
  SDA=1;
  SDA=0;
  SCL=0;
}

void   stop()
{
  SCL=0;
  SDA=0;
  SDA=1;
  SCL=1;
}

void delay(unsigned int t)
{
       while(t>0)
         {
            t--;
         }
}
```

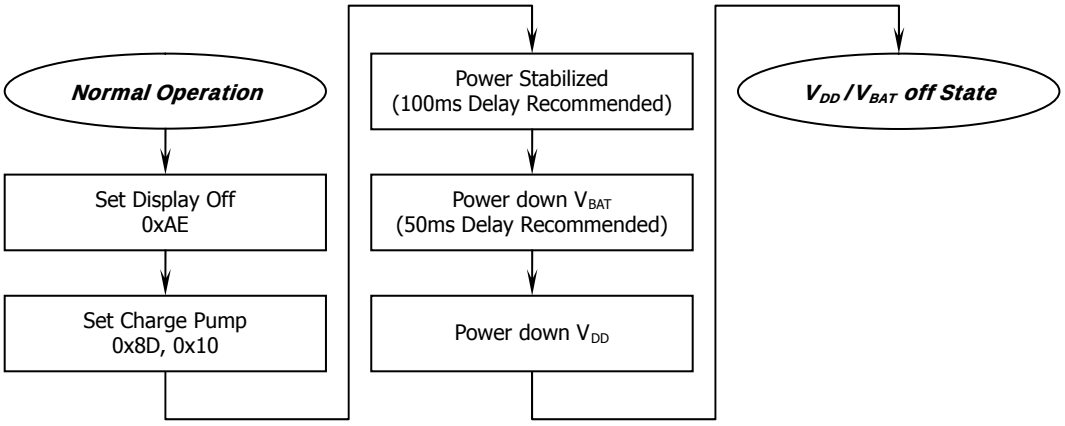
4.4.2 V_{CC} Generated by Internal DC/DC Circuit

<Power up Sequence>

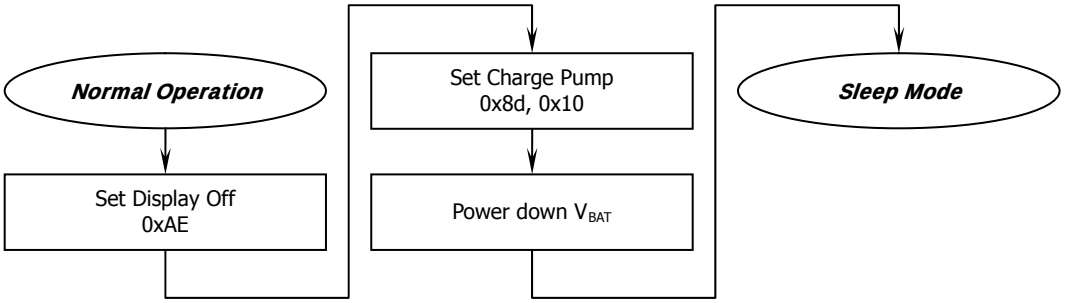


If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

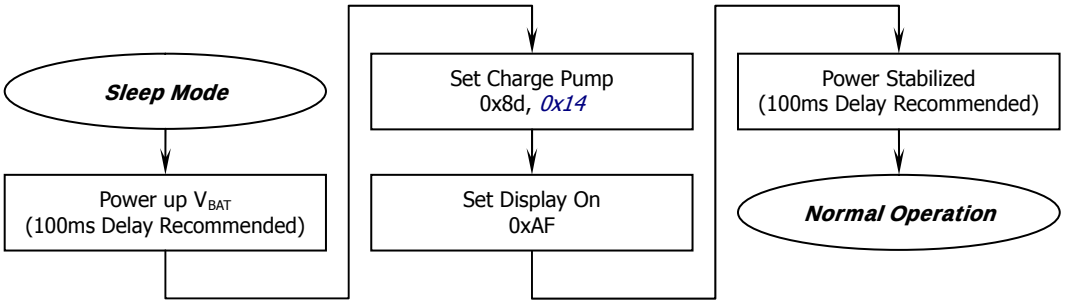
<Power down Sequence>



<Entering Sleep Mode>



<Exiting Sleep Mode>



Internal setting（Charge pump）

```
void SSD1306()
{
    RES=0;
    delay(1000);
    RES=1;
    delay(1000);

      write_i(0xAE);      /*display off*/

      write_i(0x00);      /*set lower column address*/
      write_i(0x12);      /*set higher column address*/
```

```
        write_i(0x00);      /*set display start line*/

        write_i(0xB0);      /*set page address*/

        write_i(0x81);      /*contract control*/
        write_i(0x4f);     /*128*/

        write_i(0xA1);      /*set segment remap*/

        write_i(0xA6);      /*normal / reverse*/

        write_i(0xA8);      /*multiplex ratio*/
        write_i(0x1F);      /*duty = 1/32*/

        write_i(0xC8);      /*Com scan direction*/

        write_i(0xD3);      /*set display offset*/
        write_i(0x00);

        write_i(0xD5);      /*set osc division*/
        write_i(0x80);

        write_i(0xD9);      /*set pre-charge period*/
        write_i(0x1f);

        write_i(0xDA);      /*set COM pins*/
        write_i(0x12);

        write_i(0xdb);      /*set vcomh*/
        write_i(0x40);

        write_i(0x8d);      /*set charge pump enable*/
        write_i(0x14);

        write_i(0xAF);      /*display ON*/
 }
void write_w(unsigned char dat)
{
    unsigned char m,da;
    unsigned char j;
    da=dat;
    for(j=0;j<8;j++)
    {
      m=da;
      SCL=0;
      m=m&0x80;
      if(m==0x80)
```

```
        {
          SDA=1;
        }
      else
        {
          SDA=0;
        }
      da=da<<1;
      SCL=1;
    }
    SCL=0;
    SCL=1;
}

void write_i(unsigned char ins)
{
    start();
    write_w(0x78);
    write_w(0x00);
    write_w(ins);
    stop();
}

void write_d(unsigned char dat)
{
    start();
    write_w(0x78);
    write_w(0x40);
    write_w(dat);
    stop();
}

 void   start()
{
  SCL=1;
  SDA=1;
  SDA=0;
  SCL=0;
}

void   stop()
{
  SCL=0;
  SDA=0;
  SDA=1;
  SCL=1;
}
```

```
void delay(unsigned int t)
{
      while(t>0)
        {
           t--;
        }
}
```

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C, 240 hrs	
High Temperature Storage	85°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15% RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50cm
Distance between the Panel & Eyes of the Inspector:	≥ 30cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

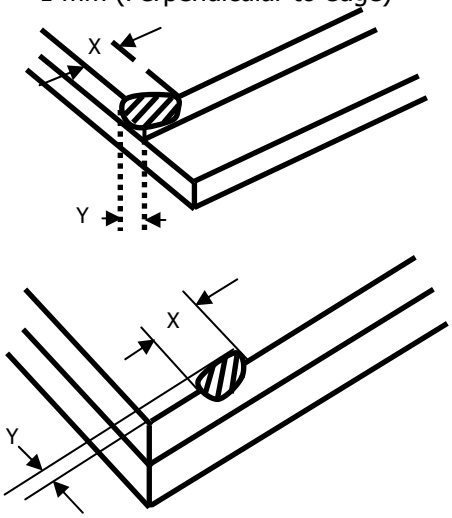
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

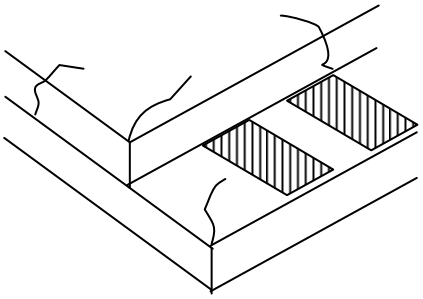
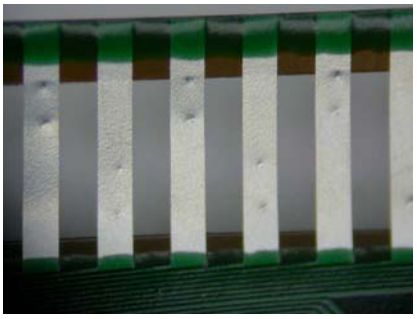
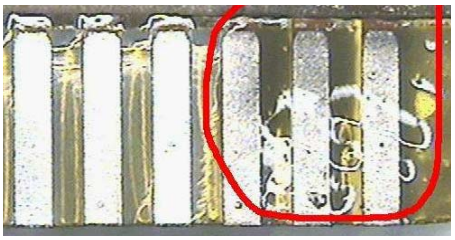
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

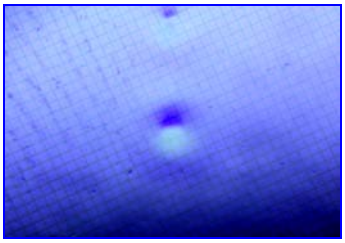
Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Copper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

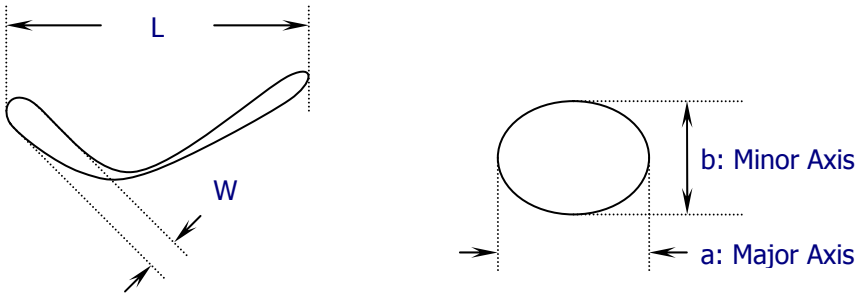
6.3.2 Cosmetic Check (Display Off) in Active Area

It is recommended to execute in clear room environment (class 10k) if actual in necessary.

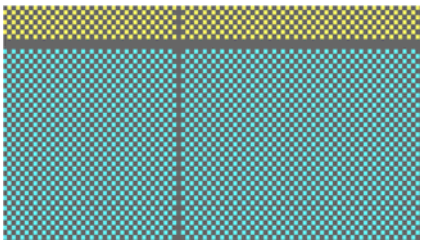
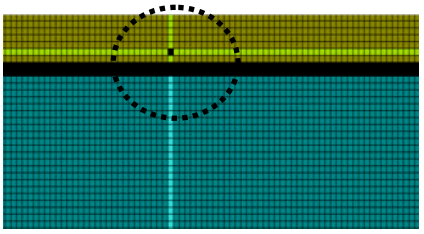
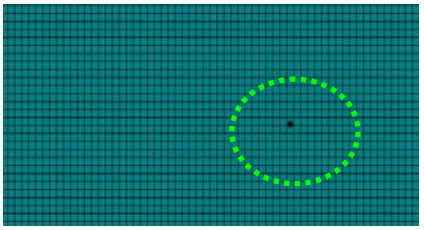
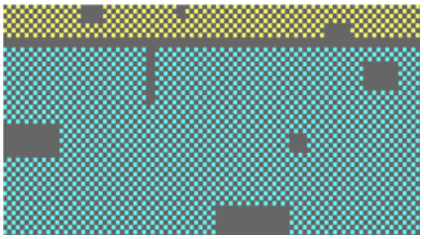
Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	W ≤ 0.1 Ignore W > 0.1 L ≤ 2 n ≤ 1 L > 2 n = 0
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major